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An evaluation of two circuit level MOSFET modules as applied to depletion-mode buried channel devices based on physical device simulation /

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AN EVALUATION OF TWO CIRCUIT-LEVEL MOSFET MODELS AS APPLIED TO DEPLETION-MODE BURIED-CHANNEL DEVICES BASED ON PHYSICAL DEVICE SIMULATION

by

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May 15th 1986
(date)

Professor in Charge

Chairman of the Department

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I would also like to express appreciation to my parents and especially to my husband, who willingly made many sacrifices throughout the course of my studies at Lehigh.

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ABSTRACT

The buried-channel (BC) MOSFET has been investigated as one possible alternative MOS transistor for VLSI applications that might avoid some of the limitations encountered in conventional surface-channel (SC) MOSFETs. Some of these limitations include carrier mobility reduction, threshold voltage fluctuations, and hot carrier injection.

There are many models available in the literature for both the conventional SC MOSFET and the BC MOSFET. Although some success has been achieved in modeling the BC MOSFET with an surface-type model, the goal of this thesis is to examine the implications of doing so. Two circuit-level models have been chosen and applied to depletion-mode BC devices. They are:

1) CSIM, a model that was developed for surface-channel devices,

but has been used for MOSFETs in general

and

2) a model that was derived exclusively for depletion-mode BC devices

as presented by White, Van de Wiele, and Lambot in 1980.

A review of the structure and operation of buried-channel transistors is followed by a qualitative discussion of the development of each model. Next, the set of parameters for each model is determined based on device characteristics obtained with MEDUSA, a physical device simulator that solves the Poisson and continuity equations in two dimensions. Input to MEDUSA is a step junction

doping profile corresponding to the conditions of constant doping in the channel region and in the bulk. There are several reasons for using device simulations rather than measurements of real devices. First, this method provides a convenient way of creating an ideal device structure, thereby satisfying some of the assumptions used in the derivation of the model. It also serves as a verifiable means of assessing how well parameters extracted from the terminal I-V characteristics compare with the inputs to the simulator, allows "noise-free" data to be obtained, and does not rely on the availability of real devices to be measured.

The results obtained suggest that both models fit the device characteristics within reasonable accuracy over the range of operation where the models can be applied and in the range of substrate bias that was used to determine the parameters. Furthermore, the BC model also correctly predicts the device behavior as a function of substrate bias. In addition, the parameters that can be related to IC process parameters, such as doping concentration, and mobility, correspond much more closely to the values supplied to the device simulator in the case of the BC model, whereas those for the CSIM model do not. Finally, a discussion of the limitations of each model is presented.

I. INTRODUCTION

A. Scope of Thesis

The goal of this thesis is to examine the implications of using a SC device model to characterize BC devices. To restrict the study, two circuit-level models, of the many available, were chosen. CSIM[1] was selected to represent SC device models. It has been used extensively at AT&T Bell Labs and has a software package, MOSPAC[2], available for parameter extraction. The model developed by White, et al.[3] was chosen to represent BC device models, because of the ease of parameter extraction even without the aid of a software package. Henceforth, this model will be referred to as the BC model.

Only large geometry n-channel devices will be studied. In addition, this work is based on physical simulation of a "software" device rather than measurements of real devices. BICEPS[4], a two-dimensional process simulation program, is used to obtain a doping profile for a typical BC device. MEDUSA[5], a two-dimensional device simulation program, is used to generate all the necessary characteristics for parameter extraction and verification of the models. It has been shown[6-8] that this technique is justified and sufficiently accurate. It also provides a convenient way of creating an ideal device structure, allows "noise-free" data to be obtained and does not rely on the availability of real devices to be measured. Fig. 1 is a flowchart showing the interaction and flow of information from process and device simulation to parameter extraction and verification that will be employed in this study.

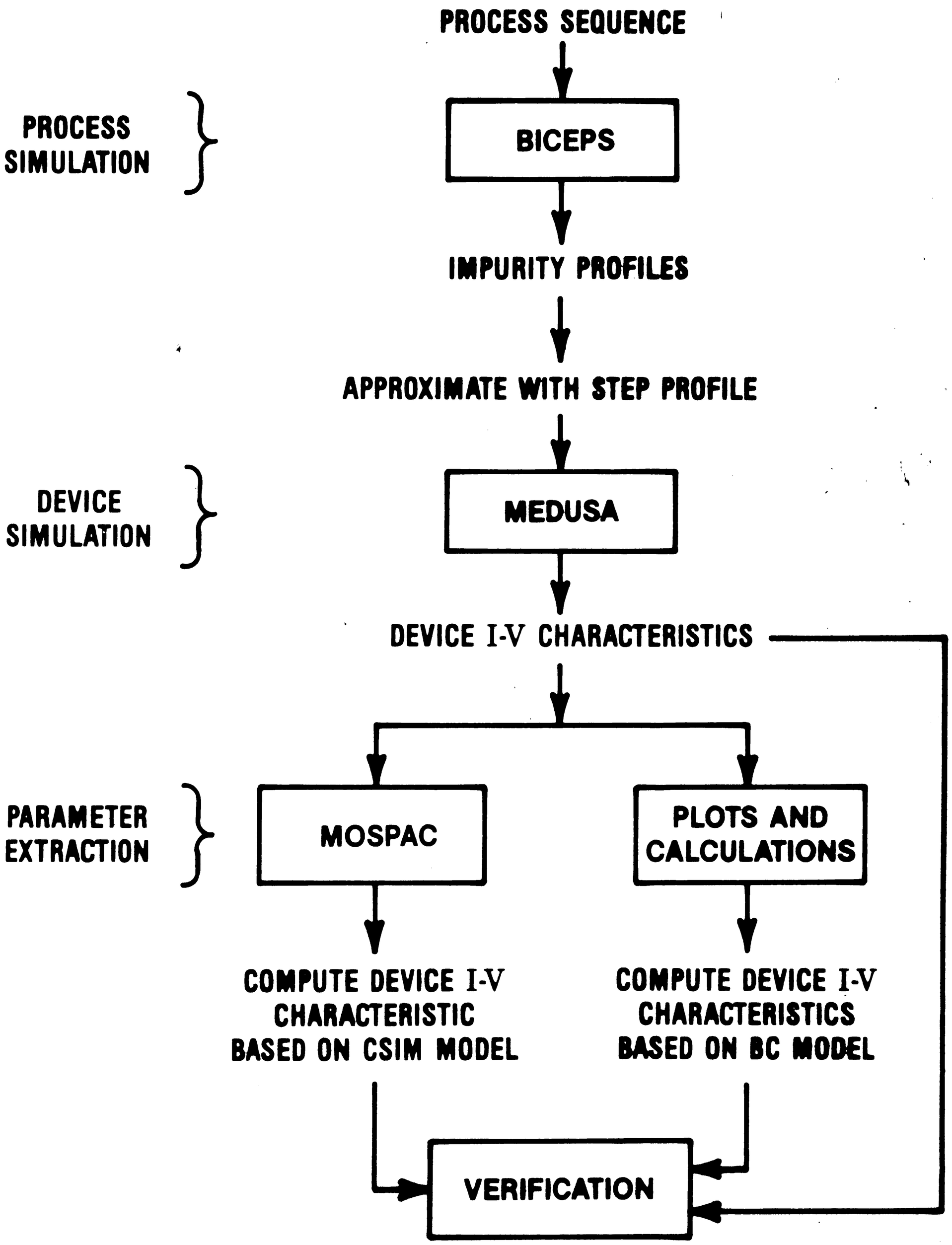


Figure 1. Flowchart - Method of Evaluation

B. History of Buried-Channel Devices

The limitations of conventional SC MOSFETs have motivated a search for new device structures. Some of these limitations include carrier mobility reduction due to surface scattering and large surface electric fields, threshold voltage fluctuations due to short channel effects, hot carrier injection due to the proximity of the channel to the gate oxide, and large 1/f noise due to interface states[9]. The BC MOSFET has been considered as one possible alternative device structure. Since the current in a BC MOSFET is restricted to the bulk silicon when biased in its depletion mode of operation, many of the above mentioned limitations can be avoided or the effects reduced.

As early as 1962, the thin-film transistor (TFT)[10], which has the n^+-n-n^+ structure from source to drain that is now known as the buried channel MOSFET, was investigated. This was followed by the study of deep depletion MOS transistors[11-12] in 1966. Similar structures known as channel-doped MOS transistors[13], ion-implanted depletion mode IGFETs[14], ion-implanted buried-channel transistors[15] and built-in channel MOSFETs[16] were also reported on. These devices all played roles as load elements in enhancement/depletion (E/D) ratio logic circuits and were typically long gate length devices. A short channel version of the BC MOSFET was suggested in 1978[17] as having potential for VLSI circuits. The claim was that this device showed low threshold sensitivities with changing gate lengths but evidence to the contrary was reported on a little later[18].

About 1981-1984, a closely related structure, known as a JMOS, or junction MOS transistor[19] was proposed. Since the implanted channel region of this device was close to the surface, carrier mobility was reduced due to high surface fields and additional surface scattering so that the current capability of this device was not significantly improved[20].

As the BC MOSFET drew attention, the need for models became apparent. Several circuit-level models for the buried-channel IGFET have emerged over the years. Some of these models will be briefly reviewed here.

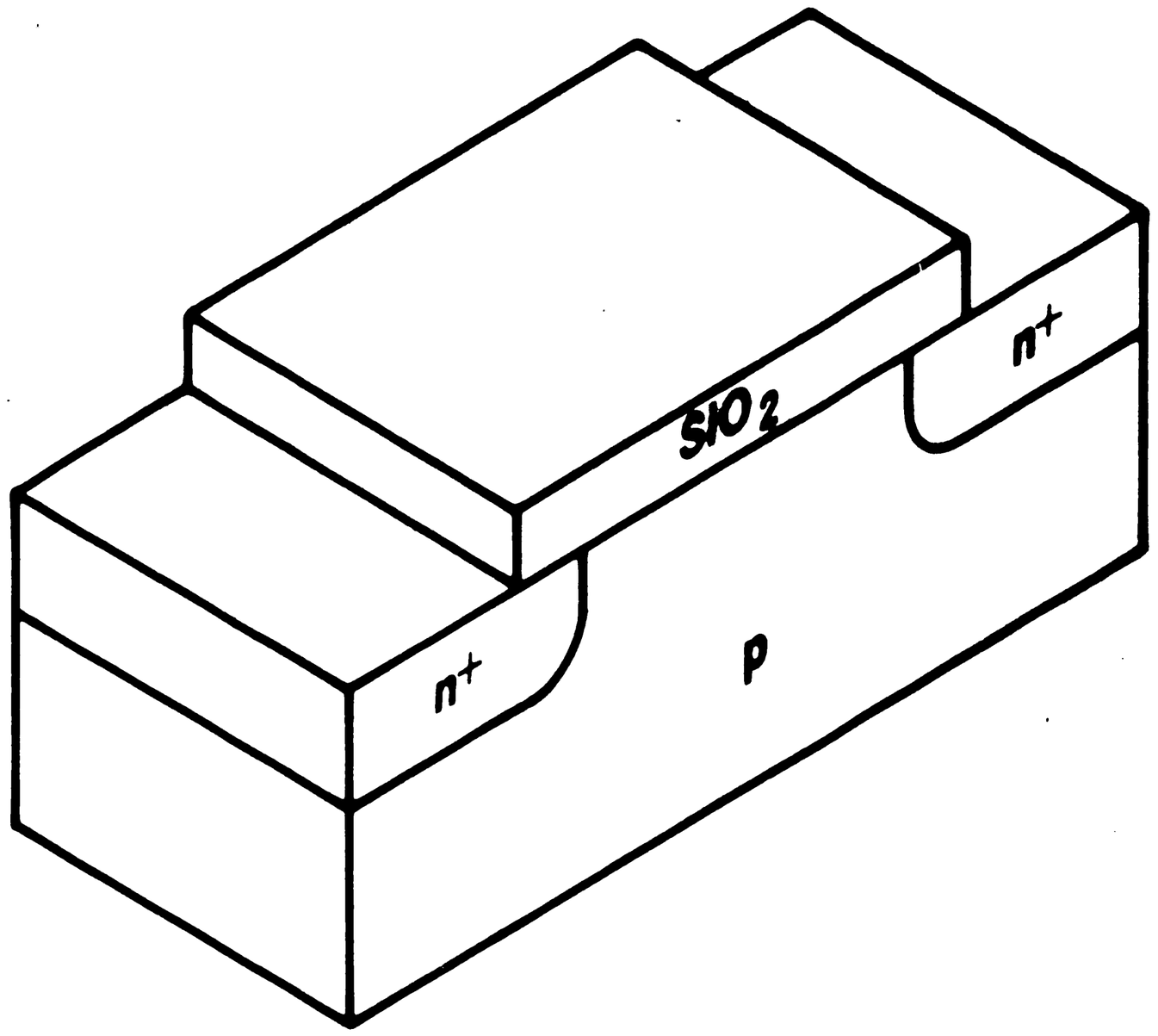
Initially, the BC device was treated essentially the same as a SC MOSFET, with an additional term added to correspond to the channel charge[21]. Since this type of model considers the implanted dose to exist as a thin sheet at the Si-SiO_2 interface, it may be satisfactory for devices with very shallow channel implants. In 1973, Edwards and Marr[22] used a step profile to approximate the gaussian profile in the channel region. Their resulting I-V equations are quite complex since they made no attempt to simplify the non-linear relationship between the gate voltage and the surface depletion width. Also, source and substrate are considered to be at the same potential and substrate bias variation is not included. Huang[23] developed much simpler I-V relations based on a constant average capacitance. Two years later, this work was extended[14] to include the substrate bias effect. In 1978, Haken[24] used a more rigorous analysis, following the work of Edwards and Marr. He added threshold voltage analysis as well as substrate bias variation. But again, the I-V

relations are quite complex, which may present a problem in terms of efficiency for circuit simulation programs. Empirical curve fitting was also tried by Wordeman[25] and Lee and Fuller[26]. In 1980, White, Van de Wiele and Lambot[3] developed another analytical model along with a simple method for determining the associated parameters. They report an accuracy of 1-3 percent with this approach. Also in 1980, El-Mansy[27] developed a four-terminal model for a depletion-mode device using simple charge-voltage relationships. He also used a step profile to estimate the channel region and develops currents and model parameters in terms of known processing data. Recently, Ma[28] introduced a model based on an equivalent circuit consisting of a MOS SC transistor, JFETs, resistors, current sources and voltage sources. The model is well suited to implementation in a circuit simulation program but does require a different equivalent circuit for each of five operation modes.

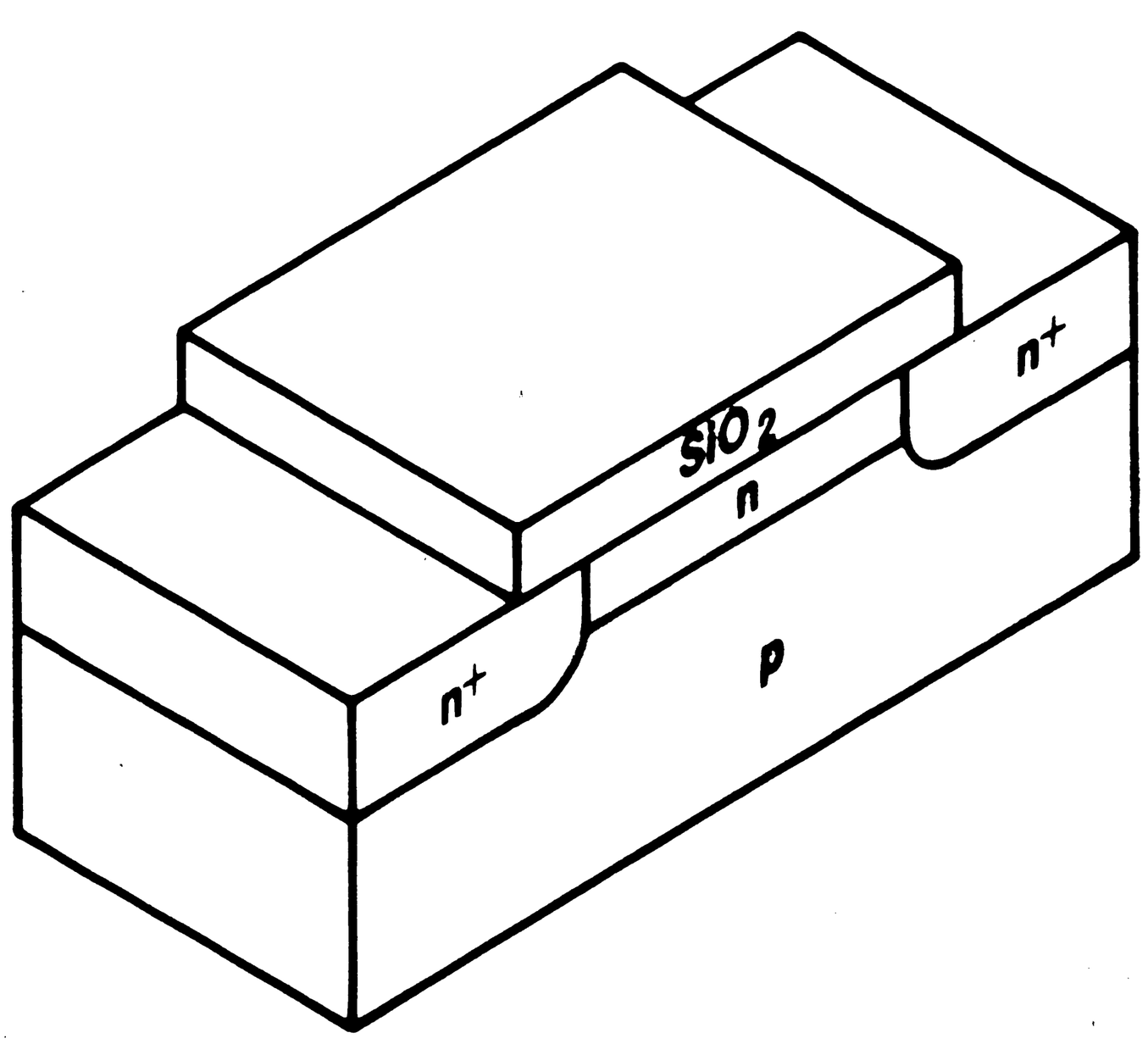
C. Definitions

The terms Surface-channel (SC), Buried-Channel (BC), Enhancement-Mode (EM), and Depletion-Mode (DM) which are used to describe the various types of MOSFETs are now defined. Only n-channel transistors will be considered here, but the situations will be analogous for p-channel devices.

Surface-channel and buried-channel devices are mutually exclusive and can be distinguished by considering the type of channel implant used to control the threshold voltage (Fig. 2). When the impurities implanted into the channel are the same type as the tub or substrate (e.g. Boron into a P-tub), a conventional MOSFET or SC device results. With this structure, the conducting channel is induced by the gate, and forms at the $Si\text{-}SiO_2$ interface, or surface of the semiconductor, via inversion. However, when the implanted impurities are of the opposite type (e.g. Phosphorus into a P-tub) and sufficiently large to create a p-n junction, a BC structure is formed. Here, the conducting channel occurs deeper into the bulk semiconductor rather than at the surface, when operating under the mechanism of depletion. Operation will be discussed in part II.



SURFACE-CHANNEL



BURIED-CHANNEL

Figure 2. Surface-Channel and Buried-Channel Device Structures

The terms enhancement-mode and depletion-mode refer to devices that are "normally off" and "normally on," respectively, at zero gate to substrate bias and can be applied to either SC or BC devices. For example, consider first an n-channel SC EM ("normally off") device. The gate voltage must be "enhanced" or increased above a particular voltage, called the threshold voltage, V_T, in order to form a conducting channel, thereby turning the device "on." The channel is actually a layer of electrons that forms by inversion of the surface when a positive gate voltage is applied. In a DM device, however, this conducting channel already exists due to the choice of gate material, when $V_{gs} = 0$, and the device is "on." To turn this device "off," the gate voltage must be reduced below the threshold voltage.

Now consider a BC EM device. For this device, we refer to a "pinch-off voltage," V_{PO}, rather than V_T. The "pinch-off voltage" is defined as the gate voltage at which the two depletion regions of the device meet, thus eliminating the channel of the device. When the gate voltage is increased above V_{PO}, a conducting channel is formed in the bulk silicon between the source and drain regions. As in the surface device, this channel exists at $V_{gs} = 0$ for the BC DM device. In order to turn the device "off" the gate voltage must be reduced, causing a depletion layer from the surface to extend into the bulk, thereby pinching off the channel.

With these definitions, it is possible to have 4 types of n-channel MOSFETs.

1) Surface-Channel Enhancement-mode

2) Surface-Channel Depletion-mode

3) Buried-Channel Enhancement-mode

4) Buried-Channel Depletion-mode

An example of the threshold characteristics (I_{DS} *vs.* V_{GS} for $V_{DS} = 0.1$ and $V_{BS} = 0$), for each of these devices is shown in Figs. 3-6. The current at $V_{GS} = 0$ is indicated by the arrow.

The work function difference, Φ_{MS}, can significantly affect the silicon surface potential of the device[29]. For an n^+-polysilicon gate, the Fermi level essentially coincides with the bottom of the conduction band, and the effective work function, Φ_M, is equal to the Si electron affinity, χ_{Si}, which is about 4.15 V. For a p^+-polysilicon gate, the Fermi level coincides with the top of the valence band, and the effective work function, Φ_M, is equal to the sum of χ_{Si} and E_g/q, which is about 5.25 V. Therefore, it is sometimes possible, depending on the channel doping, or in the case of a BC device, the thickness of the buried channel, to convert a DM device to an EM device by merely changing the gate type, thereby shifting the threshold voltage by about 1.1 volt.

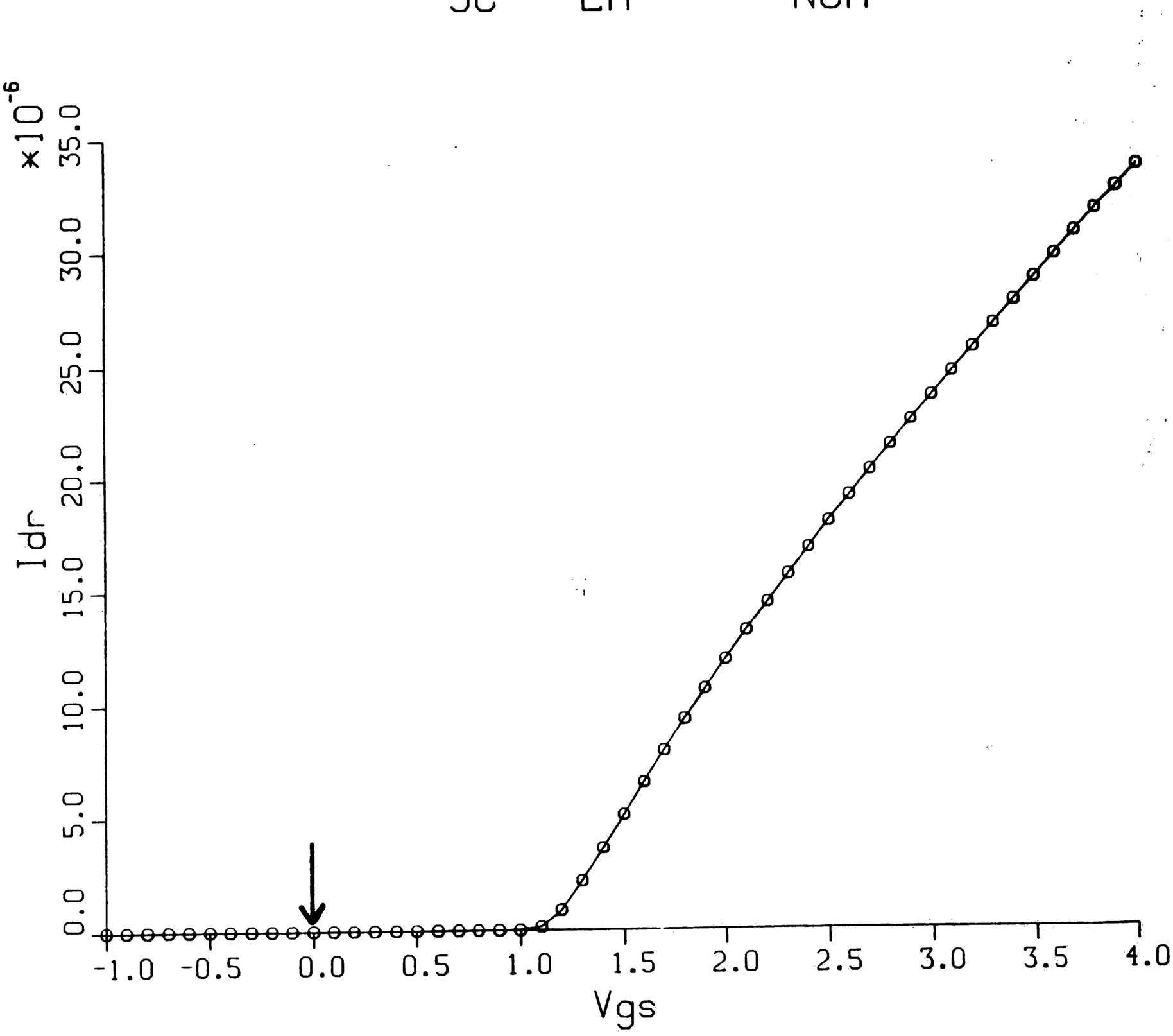


Figure 3. Threshold Characteristic for a SC EM Device

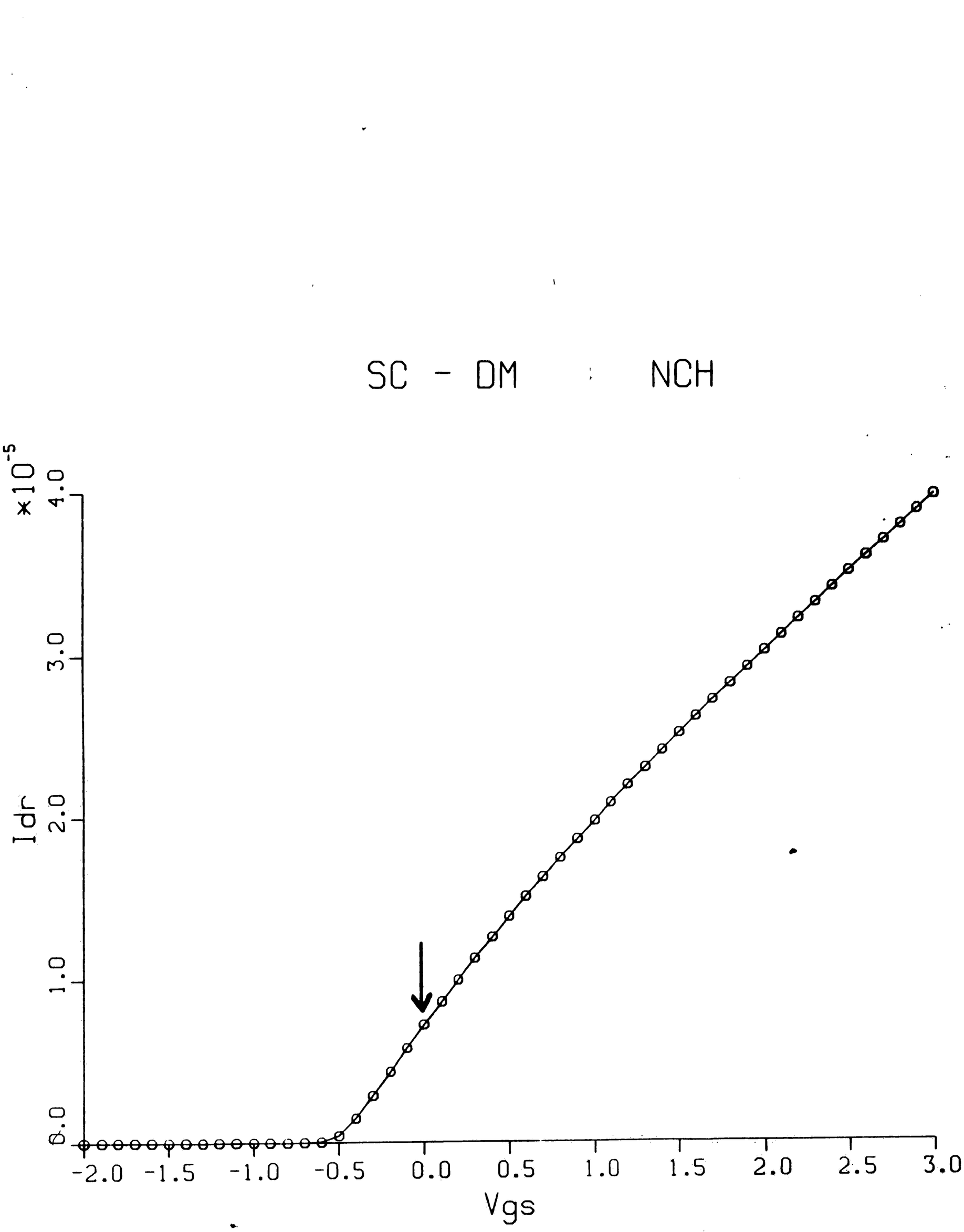


Figure 4. Threshold Characteristic for a SC DM Device

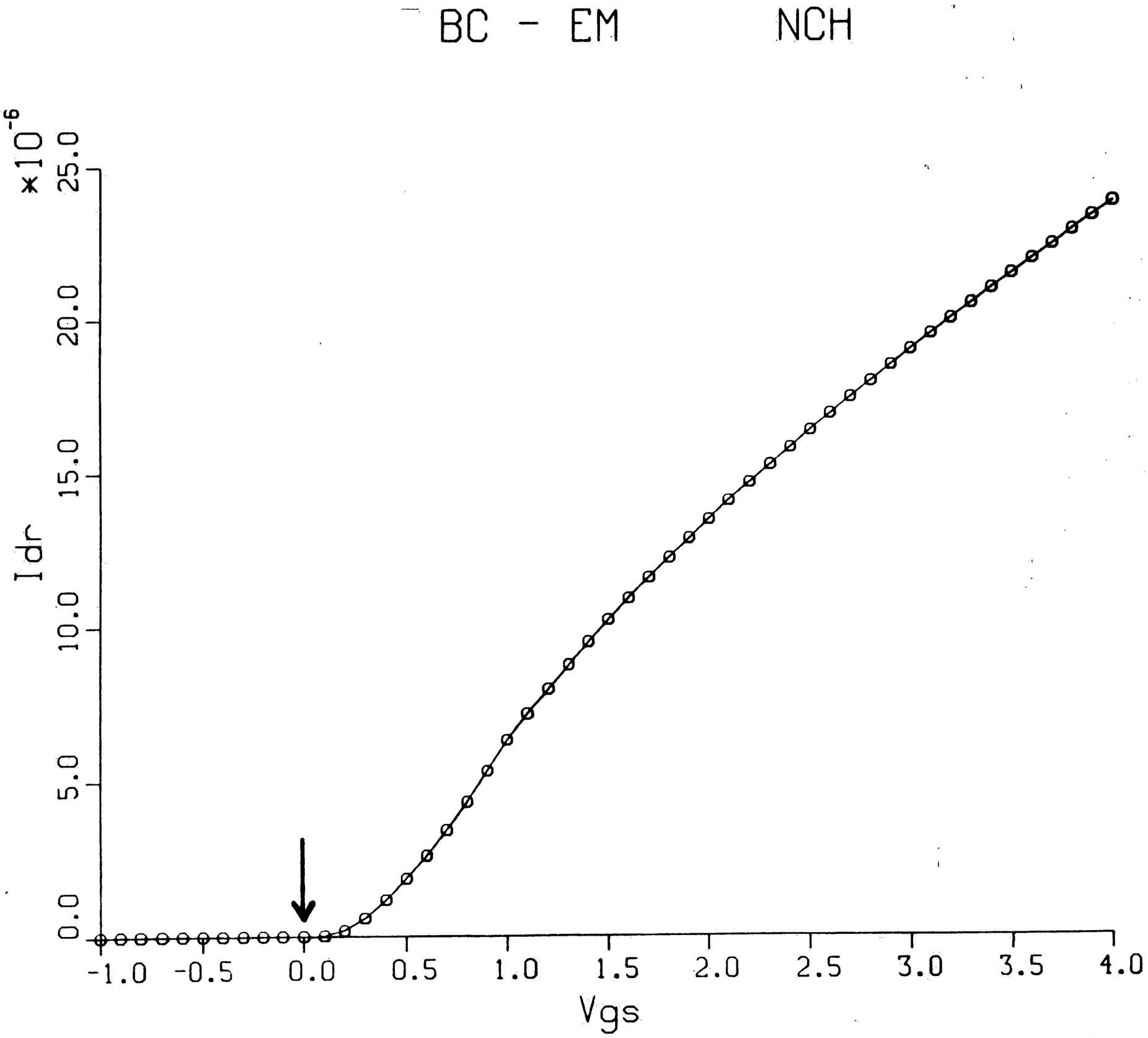


Figure 5. Threshold Characteristic for a BC EM Device

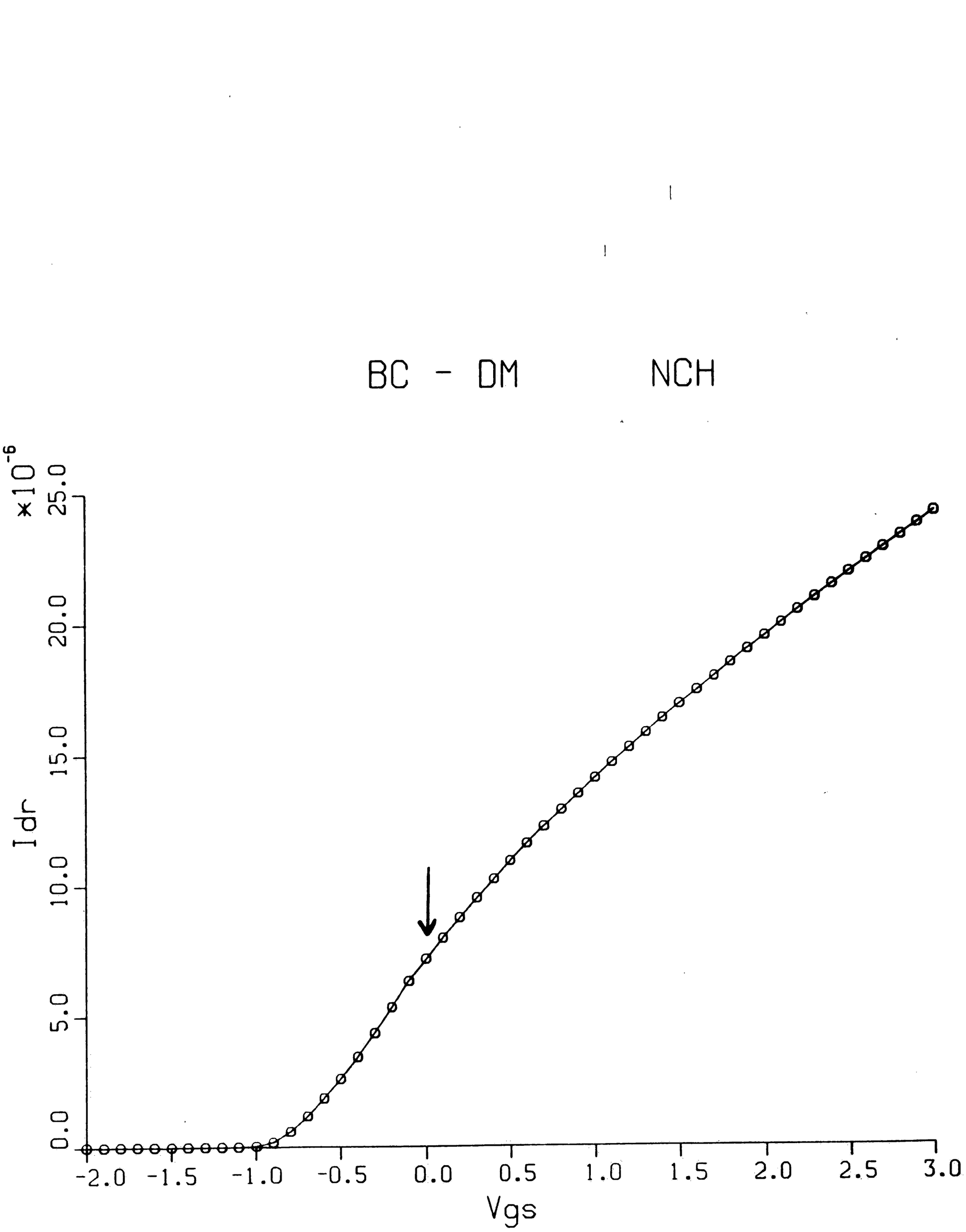


Figure 6. Threshold Characteristic for a BC DM Device

II. DEVICE STRUCTURES AND CHARACTERISTICS

The structure and operation of both SC and BC MOSFETs will be reviewed in this section. It will be useful to understand their similarities and differences when the models are reviewed in the next section.

A. Device Structures

A typical simulated doping profile in two dimensions appropriate for a buried-channel NMOS (N-channel Metal Oxide Semiconductor) device is shown in Fig. 7. Arsenic or phosphorus can be used to form the channel region which extends to a depth of about .275 μm with a peak surface concentration of about $3x10^{17}/cm^3$. In this process, there is also a deep boron implant positioned below the channel region which can be tailored to control such device properties as punch-through resistance and subthreshold swing[30]. Fig. 8 shows the one-dimensional profile through the channel region. Arsenic is used to form the source/drain regions which are driven to a depth of about .325 μm with a peak surface concentration of $1.75x10^{20}/cm^3$. Fig. 9 shows the one-dimensional profile through the source/drain region.

In contrast, Figs. 10-12 show a simulated two-dimensional profile along with the one-dimensional cuts through the channel and source/drain regions for a typical surface-channel NMOS device. Here, boron is used for the threshold adjust implant which raises the acceptor concentration near the $Si\text{-}SiO_2$ interface under the gate. The source/drain regions are similar to the BC device.

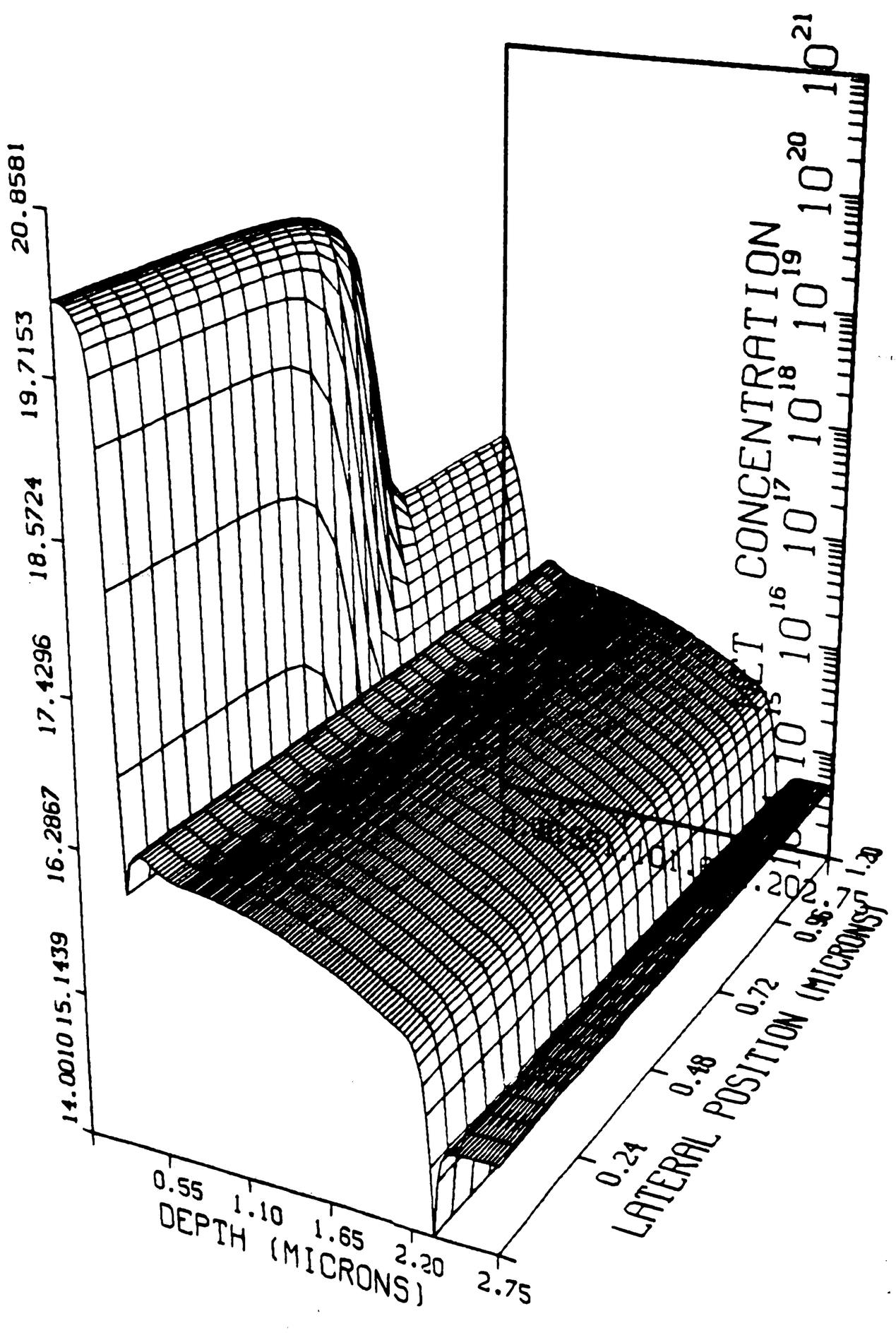


Figure 7. 2D Profile of a BC Device

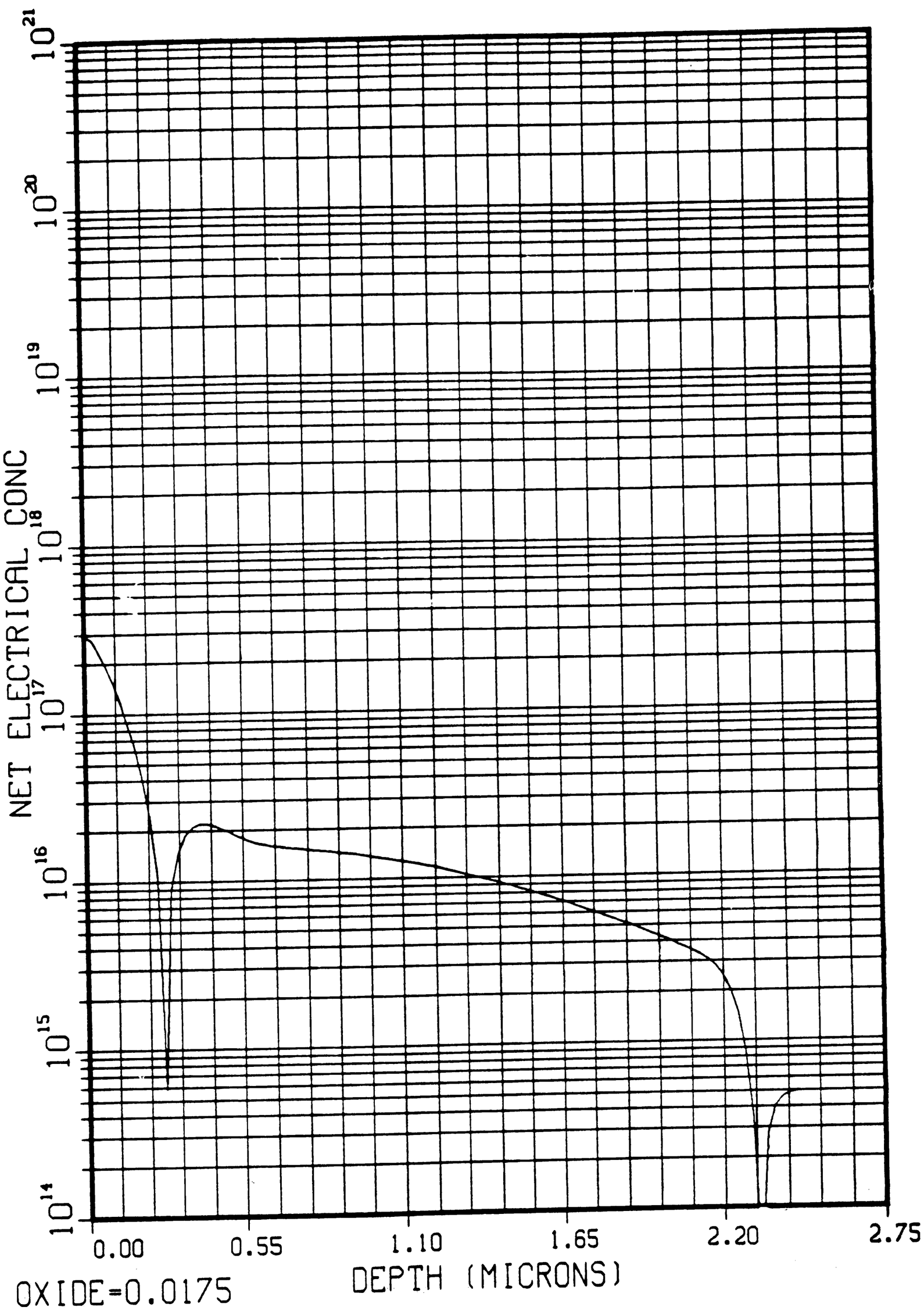


Figure 8. 1D Profile through the Channel of a BC Device

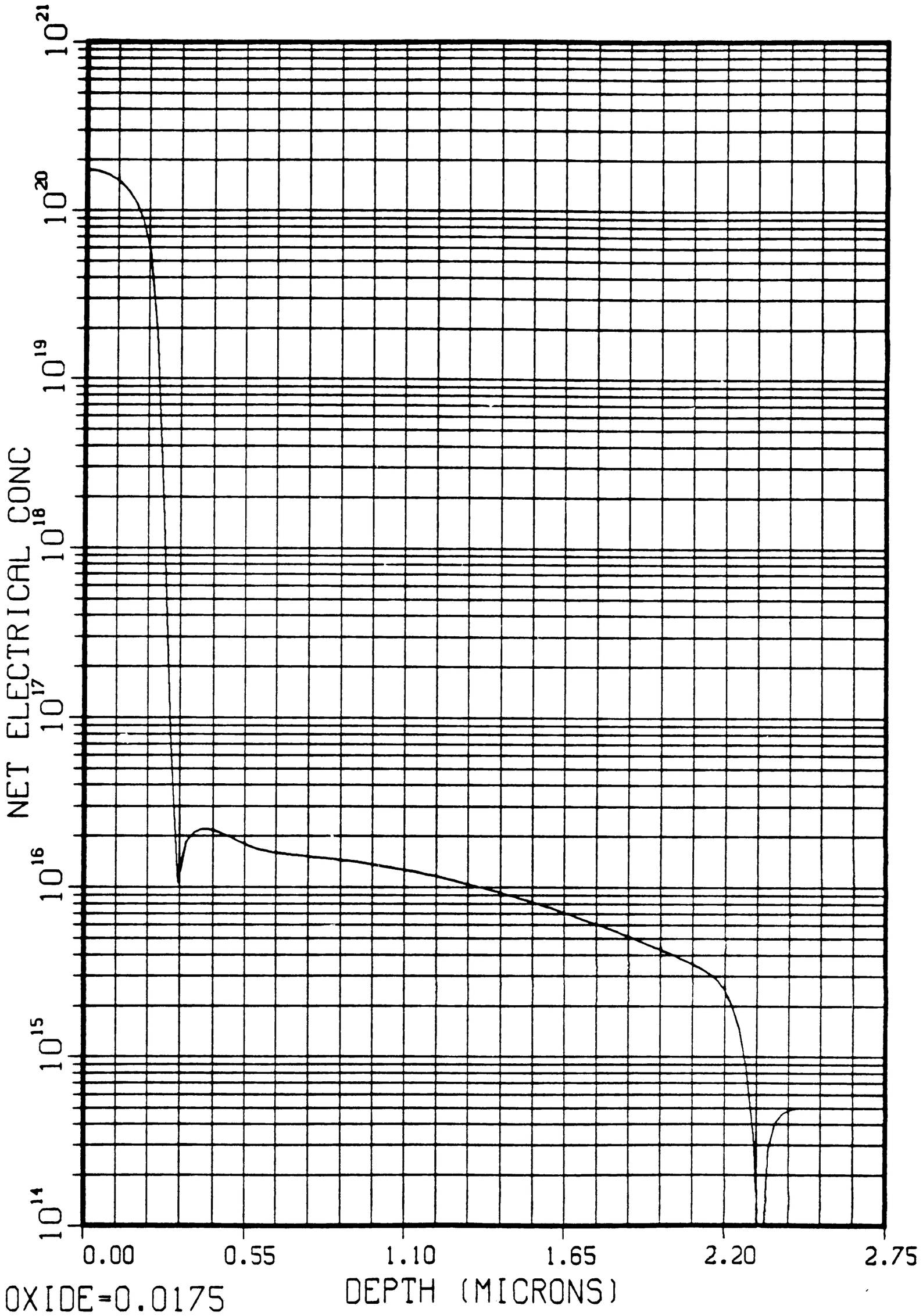


Figure 9. 1D Profile through the Source/Drain Region of a BC Device

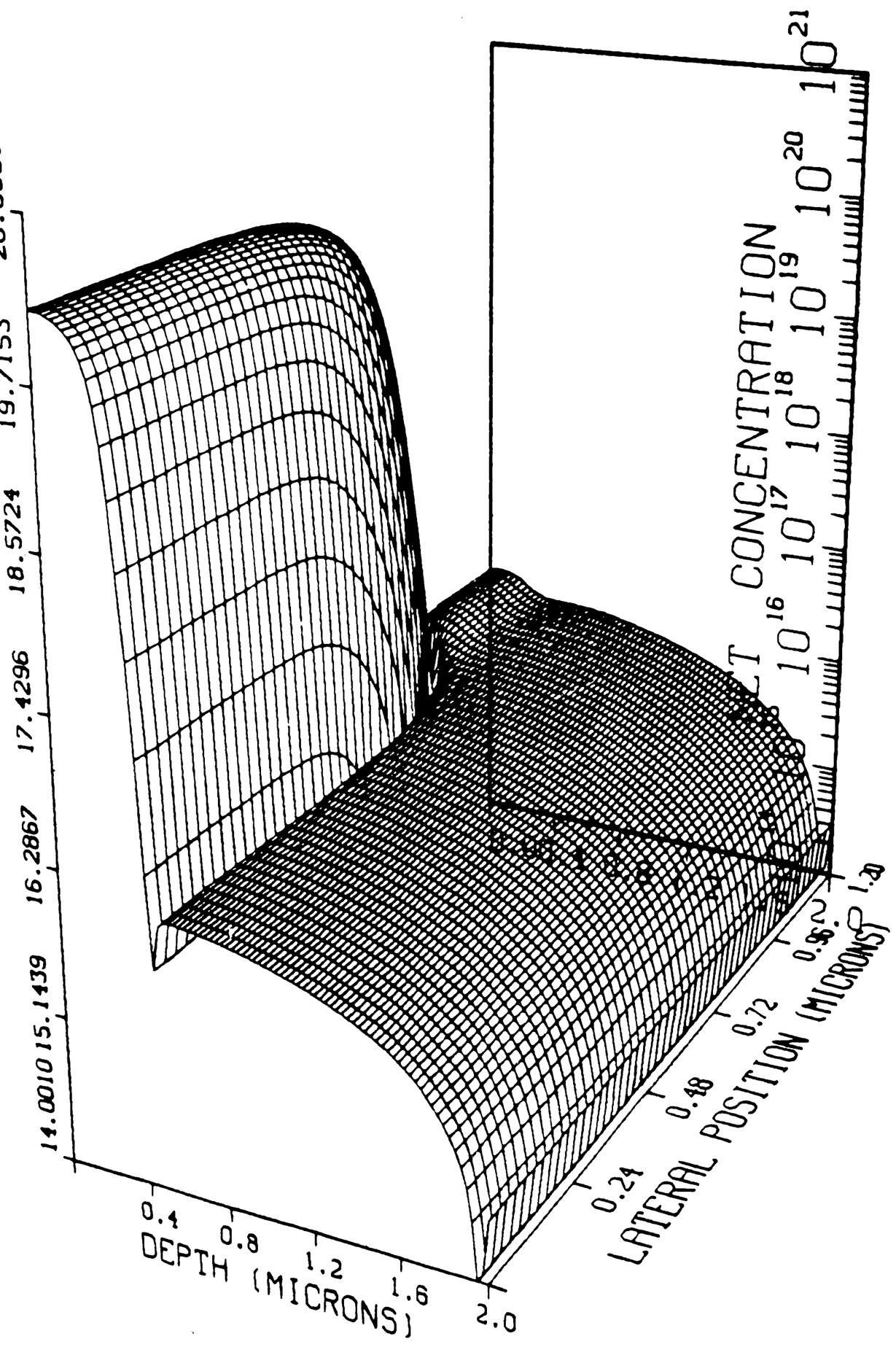


Figure 10. 2D Profile of a SC Device

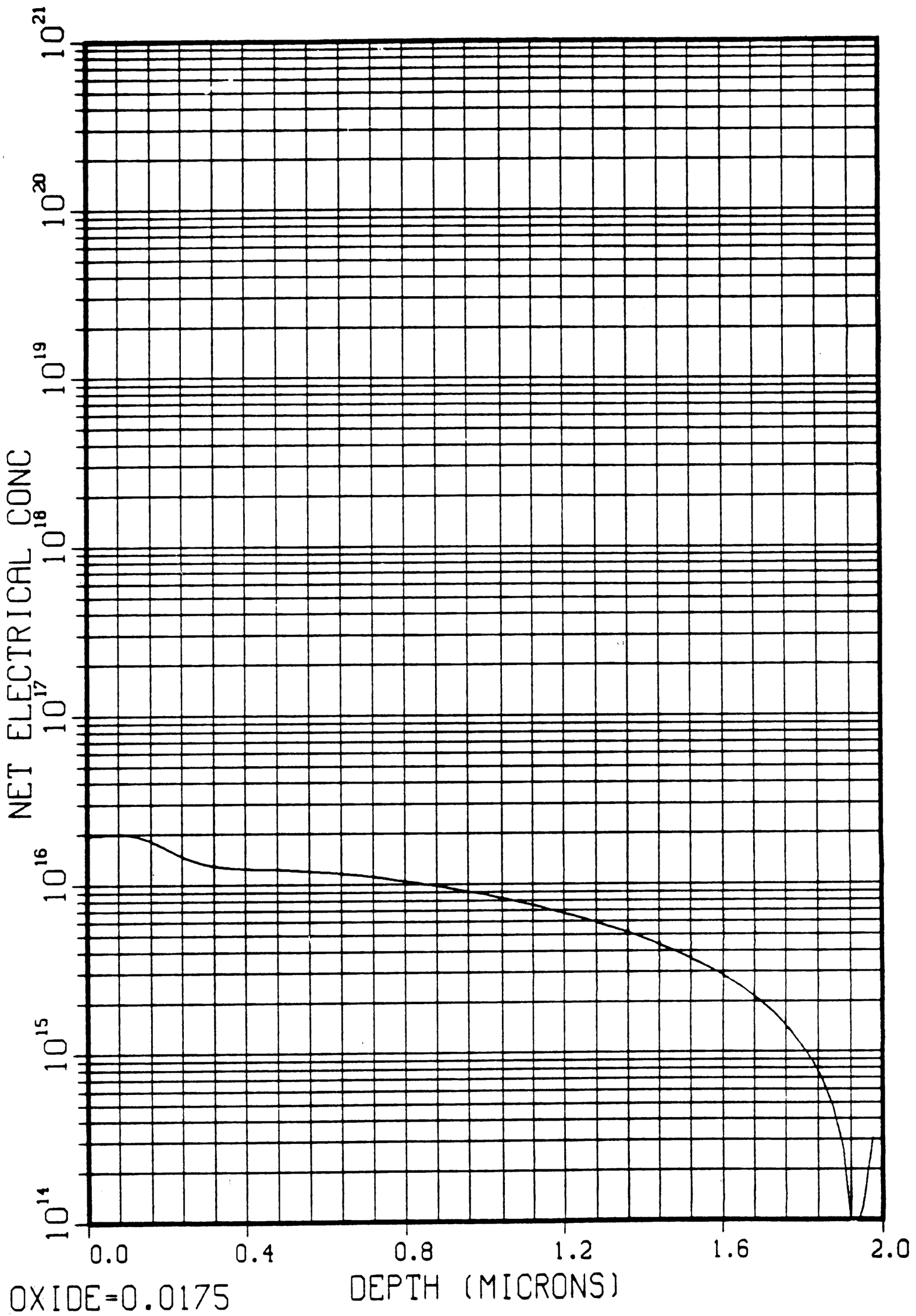


Figure 11. 1D Profile through the Channel of a SC Device

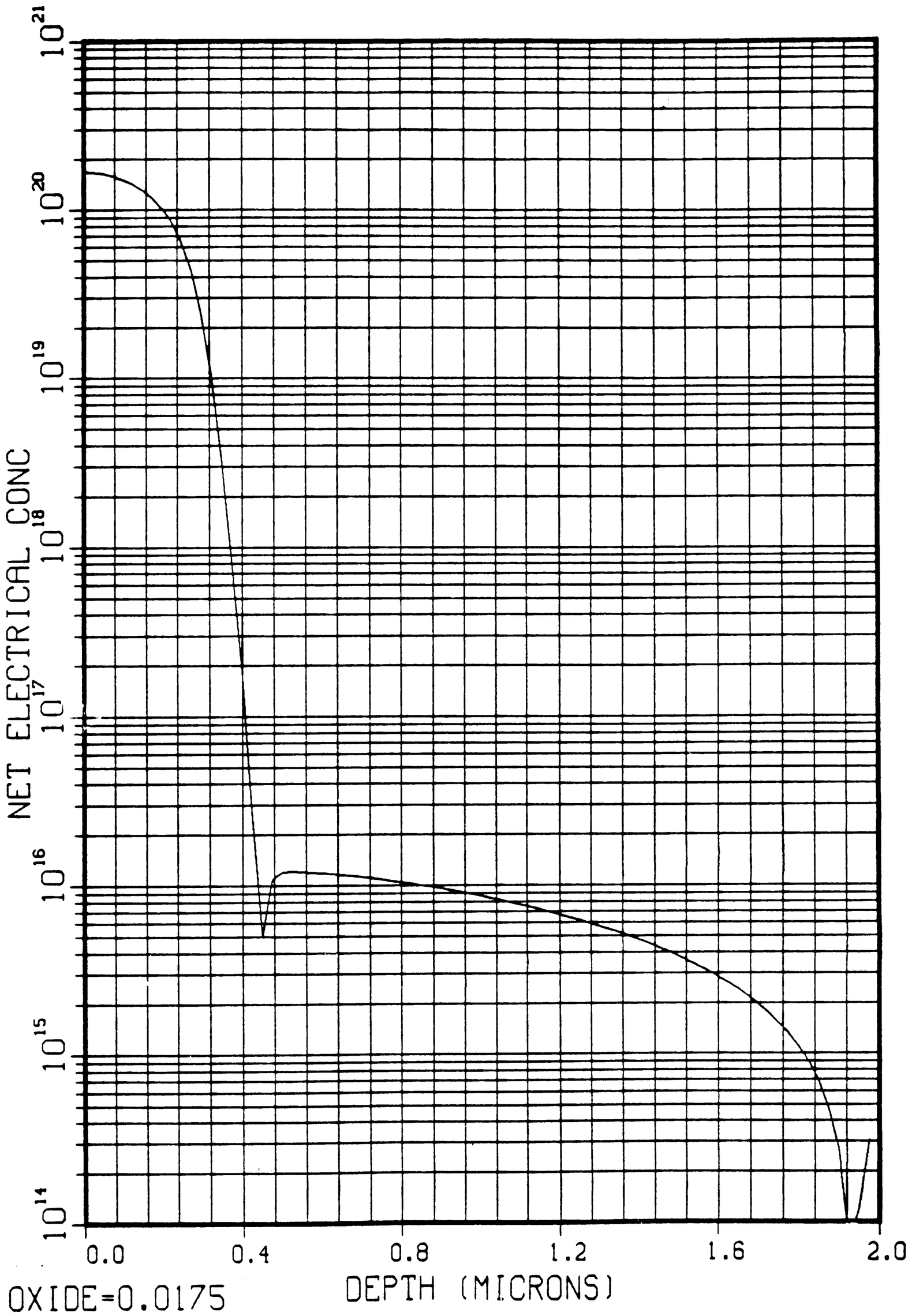


Figure 12. 1D Profile through the Source/Drain Region of a SC Device

B. Device Operation

1. SC Device

The basic structure of an n-channel SC MOSFET along with its energy band diagram is illustrated in Fig. 13. For this discussion, the source contact will be the reference voltage. The substrate can be at ground or reverse biased. When a voltage greater than V_T is applied to the gate terminal, the device is in strong inversion, i.e., an inversion layer of electrons forms at the semiconductor surface between the two n^+ regions. Current can flow through this conducting channel when a voltage is applied to the drain. Variations in the gate voltage modulate the conductance of the surface channel region.

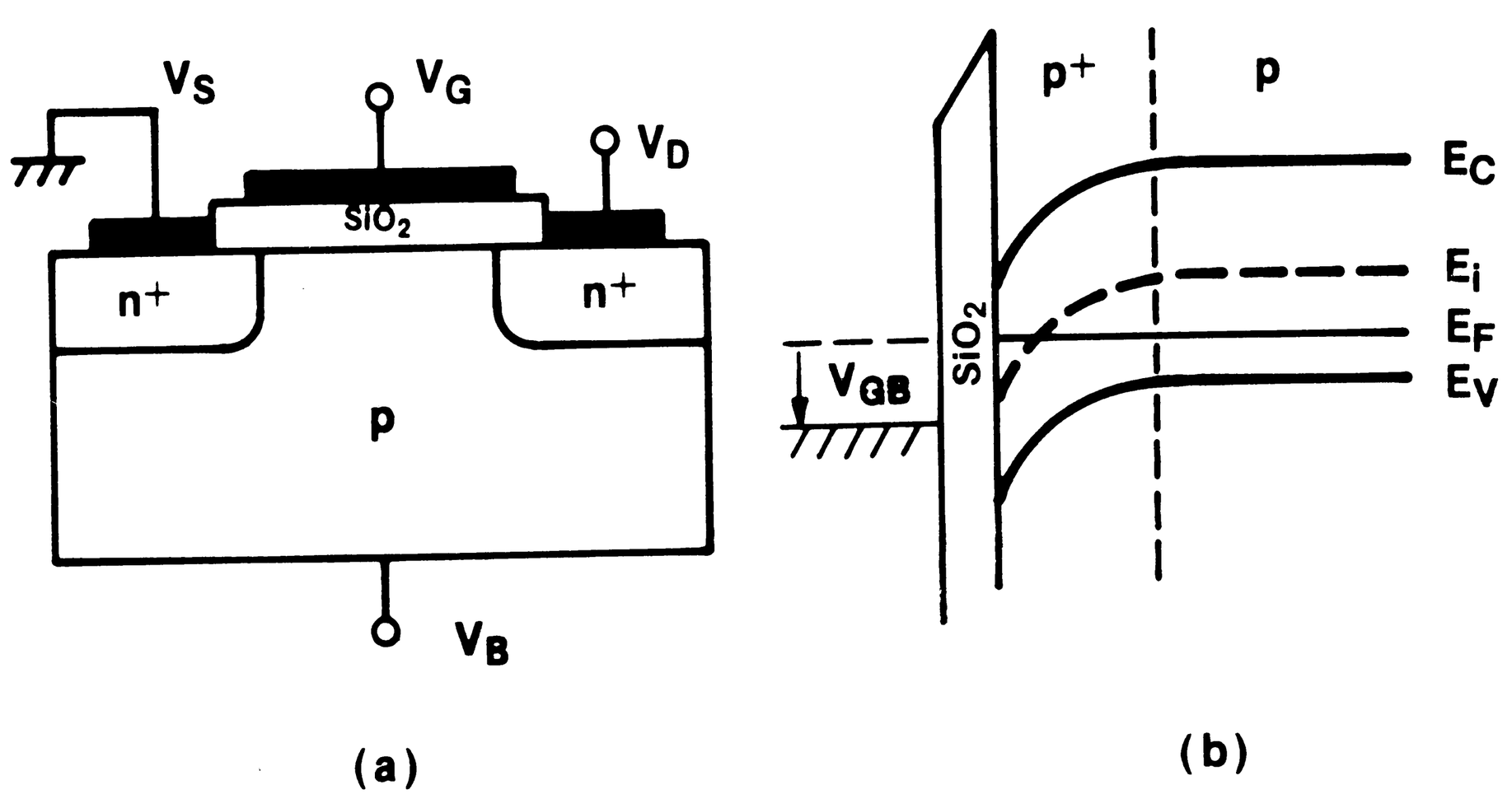


Figure 13. (a) SC MOSFET, (b) Energy Band Diagram

A mode of operation which is important for low voltage, low power applications is known as subthreshold conduction. For gate voltages below V_T, a weak inversion region exists at the surface and a small current flows by the mechanism of diffusion. Fig. 14 shows the MOSFET as operated in the linear or triode region (low drain voltage). In this mode of operation ($V_G > V_T$), the current is proportional to the drain voltage.

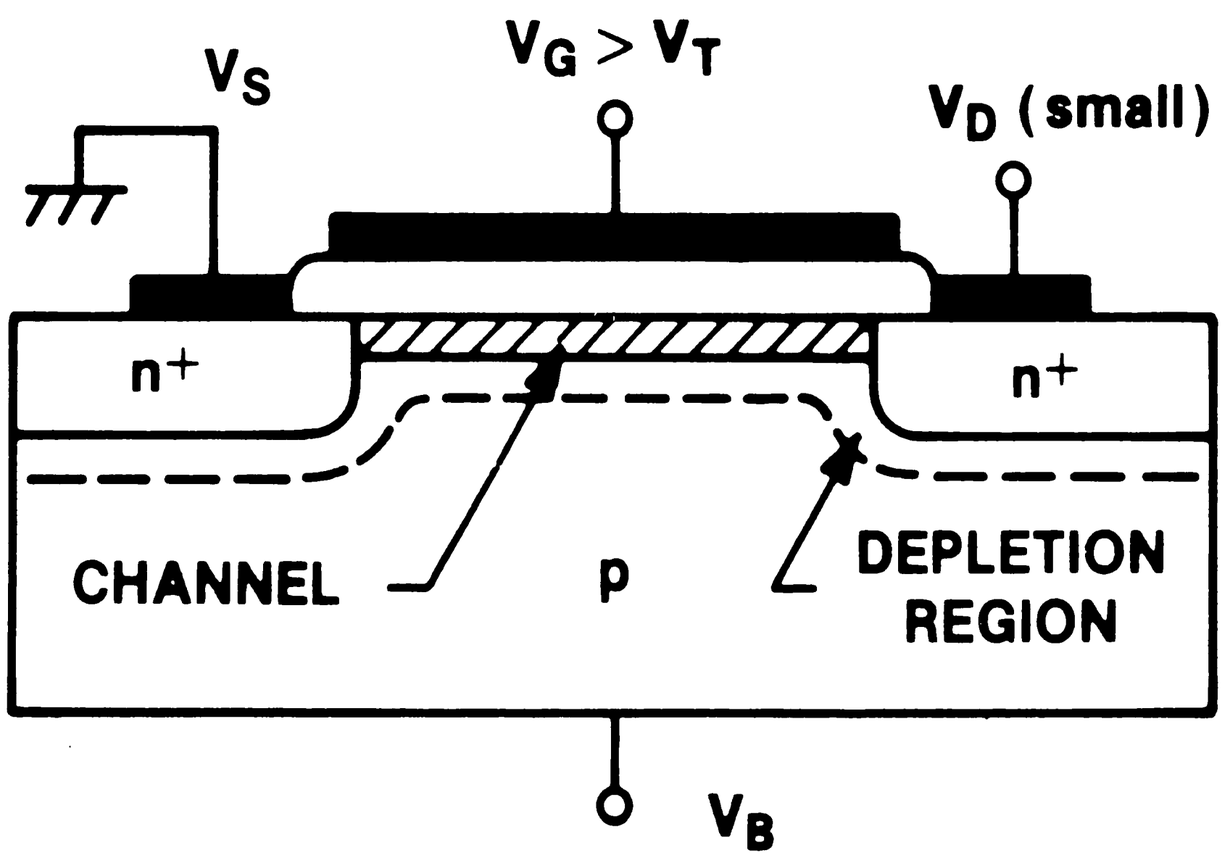


Figure 14. SC MOSFET Operated in the Linear Region

For larger drain voltages, the channel begins to narrow at the drain end until it becomes "pinched off" at a voltage referred to as V_{SAT}. (See Fig. 15). Beyond this point, the device is said to be in its saturation mode of operation where the current remains essentially the same. For $V_D > V_{SAT}$, the effective channel length is reduced, as shown in Fig. 16, and the electrons are swept across the depletion region by the high electric field.

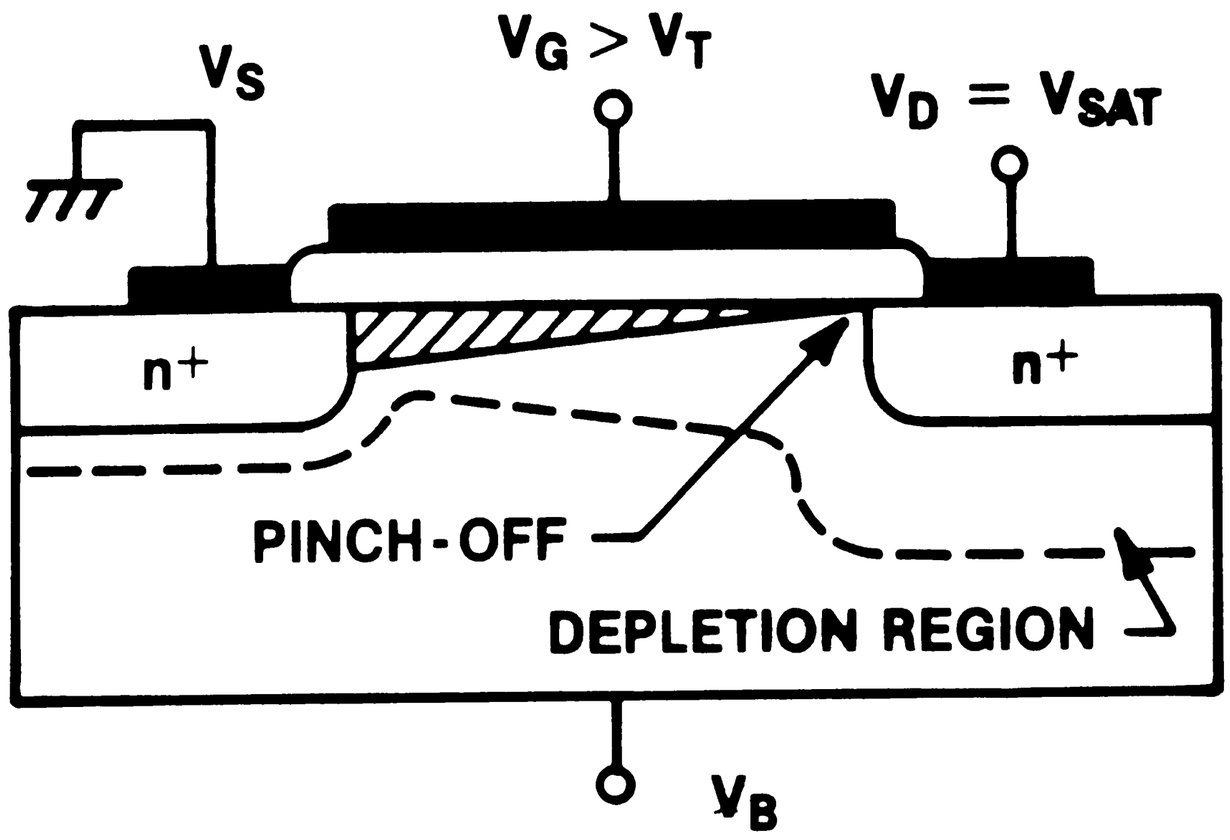


Figure 15. SC MOSFET at Pinch-Off

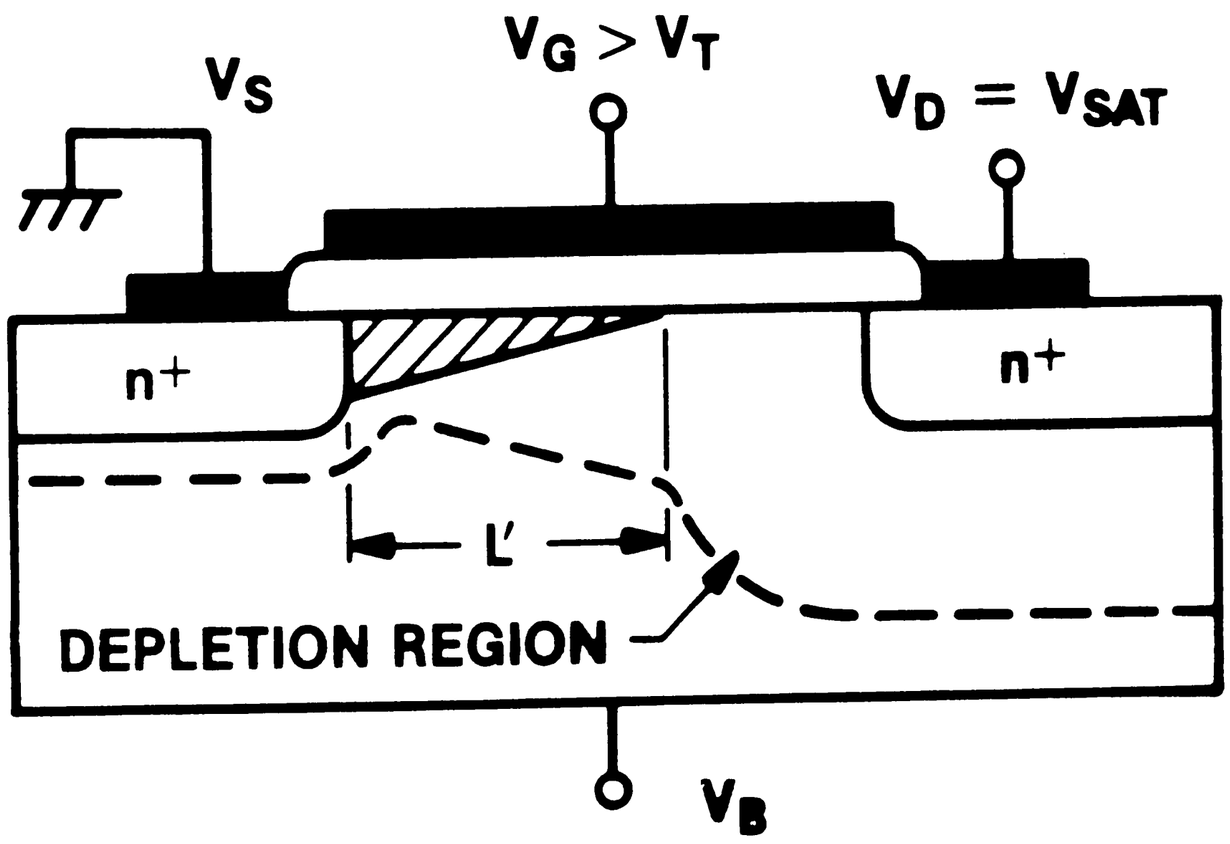


Figure 16. SC MOSFET Beyond Saturation

In all modes of operation, the carrier mobility is reduced due to the surface electric field and surface scattering mechanisms. This effect is most apparent at higher gate voltages, since the surface field becomes significant and the electron distribution moves closer to the $Si\text{-}SiO_2$ interface. Figs. 17-19 show typical I-V plots for the SC EM device.

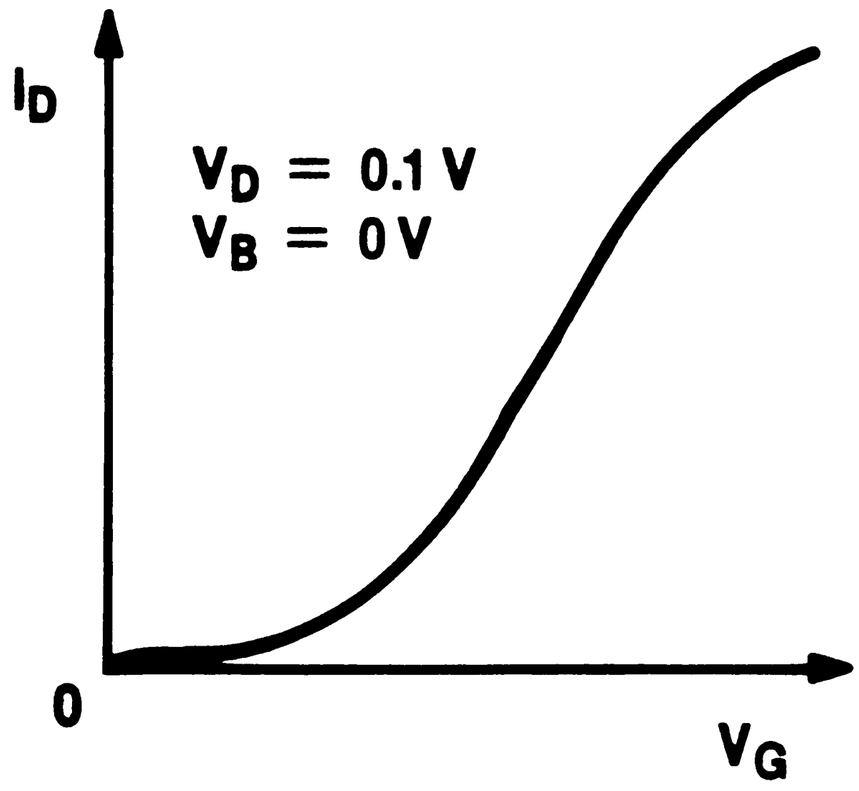


Figure 17. Threshold Characteristic of a SC EM Device

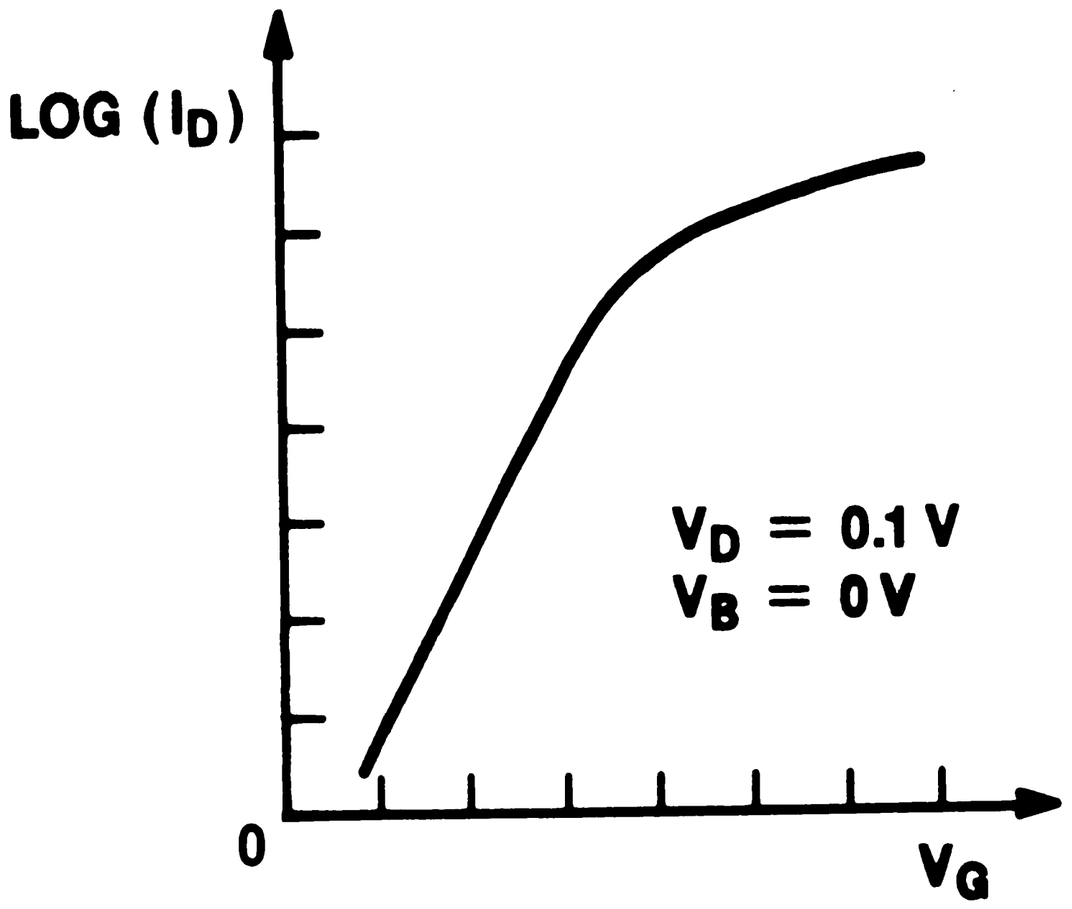


Figure 18. Subthreshold Characteristic of a SC EM Device

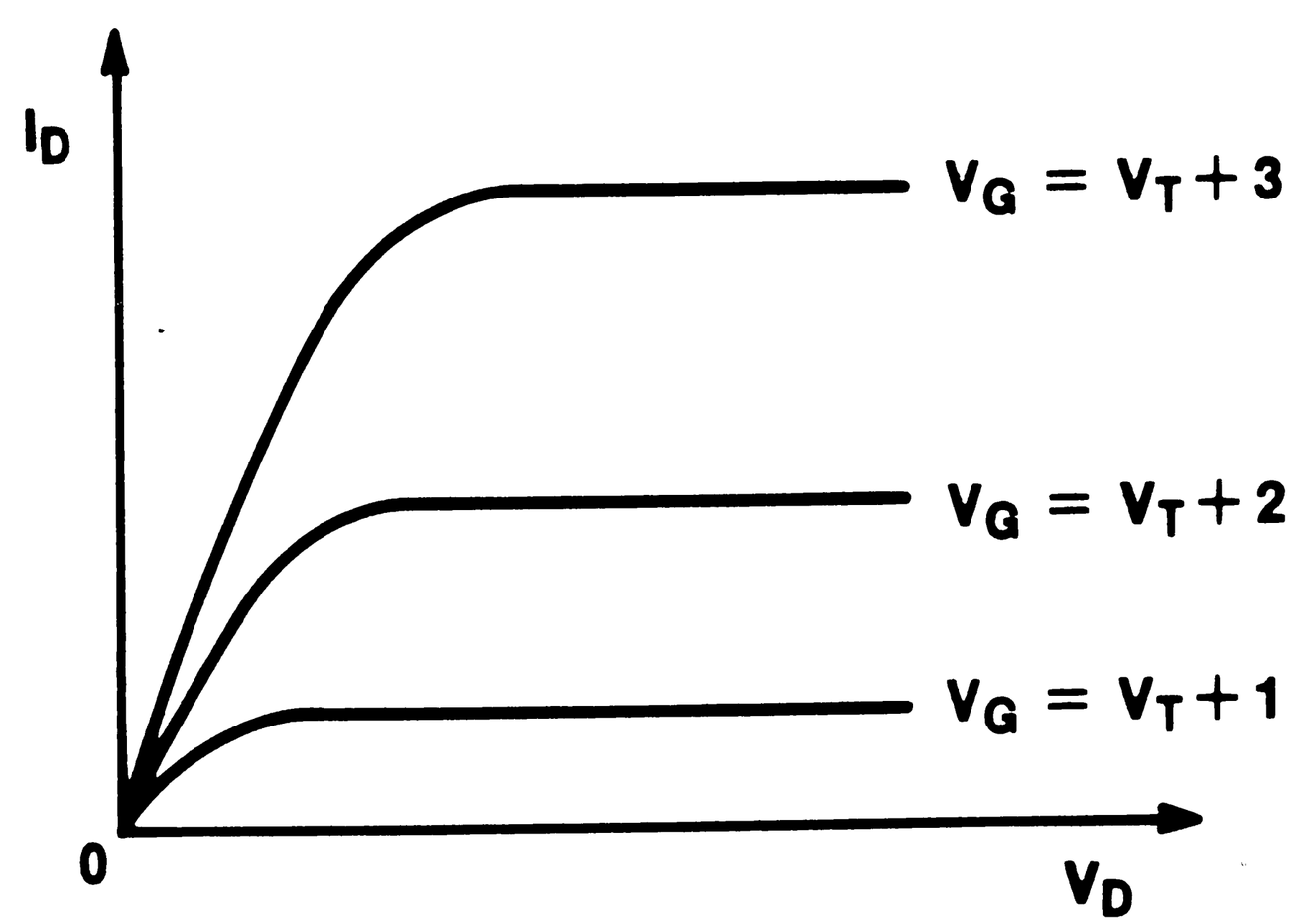


Figure 19. Output (Drain) Characteristic of a SC EM Device

2. BC Device

The basic structure of an n-channel BC transistor along with its energy band diagram is illustrated in Fig. 20. The width of the indicated depletion regions is controlled by the applied voltages: the gate voltage, V_G, modulates the channel from the surface side while the substrate or backgate voltage, V_B, modulates the channel around the junction depth, x_j. The conduction of the device is directly related to the size of the channel between these two depletion regions. It should be noted that for the case of an n-channel device, as indicated, an increasing gate voltage will reduce the surface depletion width, hence increase the current.

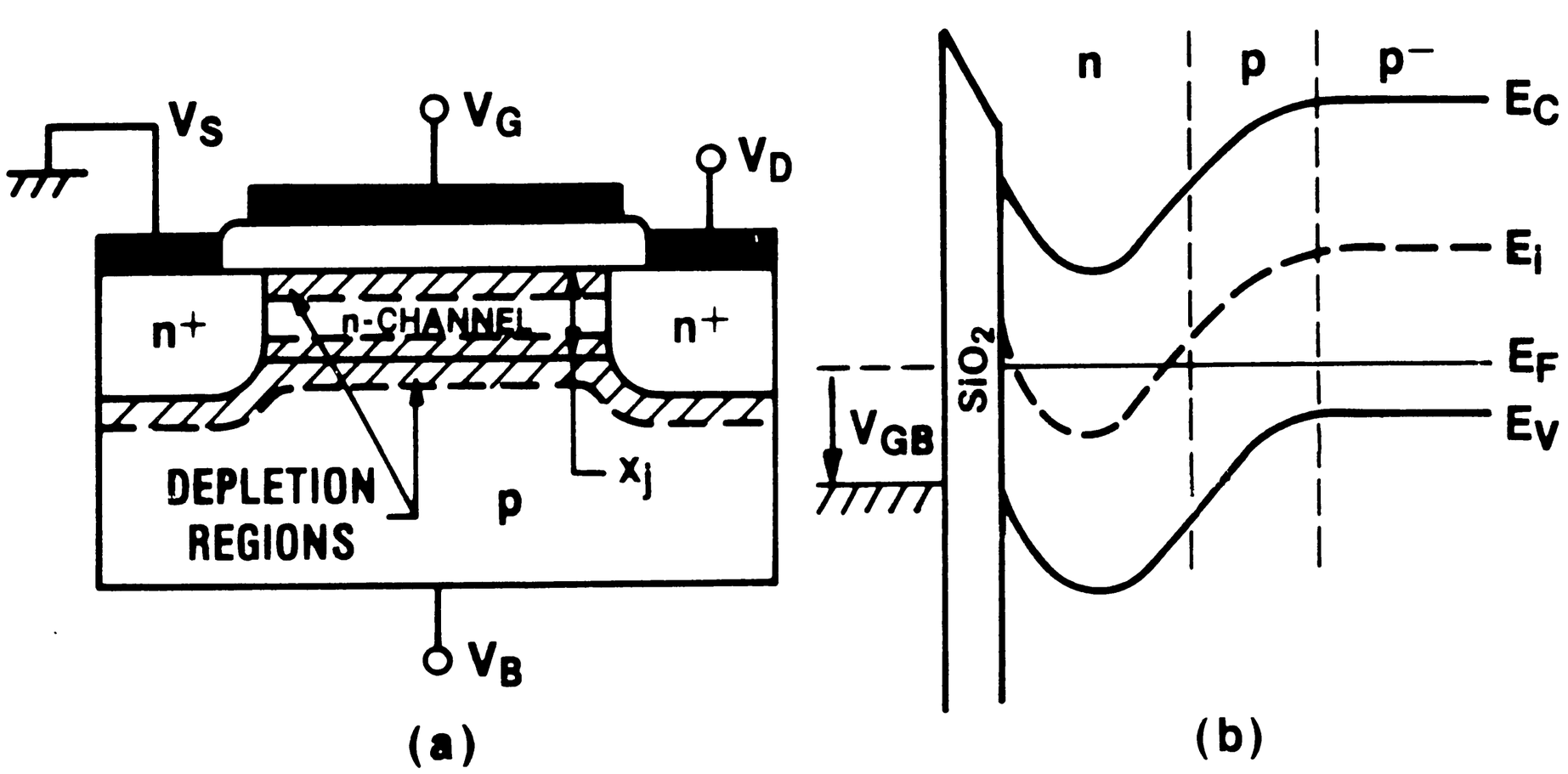


Figure 20. (a) BC MOSFET, (b) Energy Band Diagram

Several operating modes can be considered[31]. For large negative gate voltages, two situations can occur, depending on the thickness of the channel, the channel doping and the applied substrate bias. In some devices, the surface depletion layer touches the bulk depletion region, thus pinching off the channel so that no current can flow as shown in Fig. 21(a). For devices with deeper channels and/or higher doping, and at small values of substrate bias, the maximum depletion width due to the gate bias is reached before the two depletion regions meet as in Fig. 21(b).

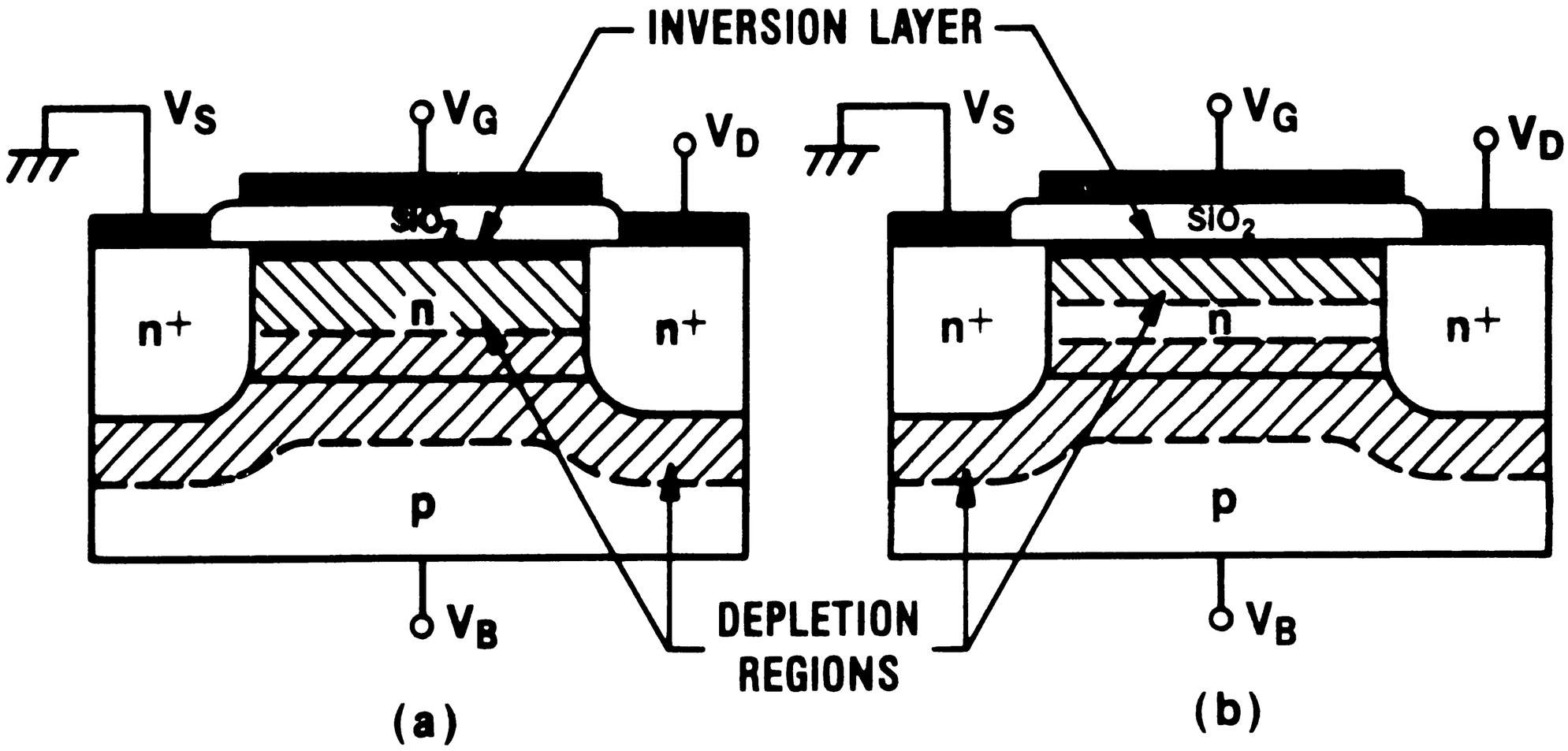


Figure 21. BC MOSFET Operated in the Inversion Mode: (a) Channel Pinched Off, (b) Channel Not Pinched Off"

In this situation, the channel cannot be pinched off unless a large negative substrate bias is applied. The consequence of an even larger negative gate voltage is an inversion layer of holes which forms at the surface of the device, but

the current remains essentially the same; holes do not affect the conduction. This is known as the inversion mode of operation. It should be noted that the n^+ source/drain regions as well as the n channel region are implanted into p-type Si. The inversion layer of holes, then, is formed by a parasitic p-n-p across the width of the device. Thus the surface potential is "pinned" by the substrate.

As the gate bias is increased beyond V_{PO}, the channel widens in the bulk silicon and a larger current is allowed to flow. This is illustrated in Fig. 22 and is known as the depletion mode of operation.

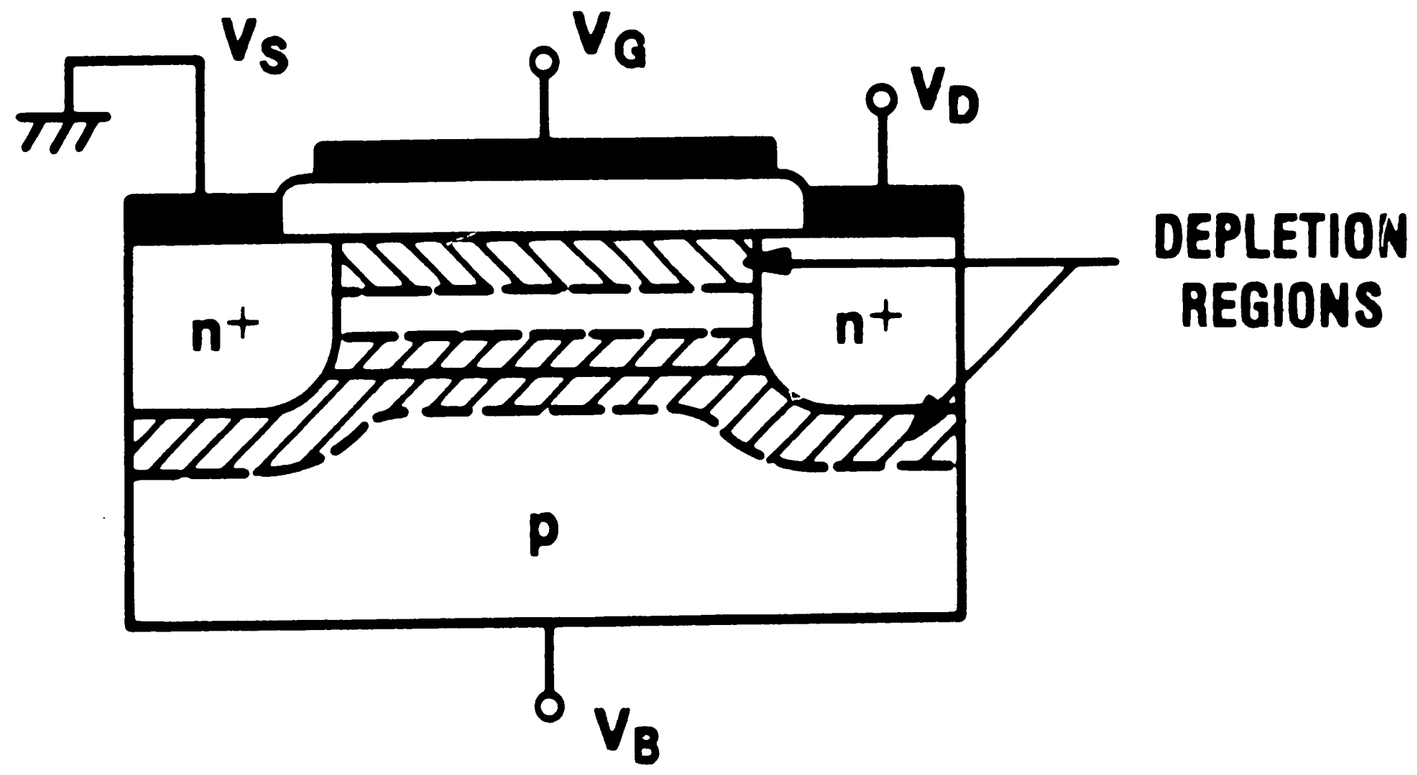


Figure 22. BC MOSFET Operated in the Depletion Mode

It is this mode of operation that makes the BC MOSFET an attractive alternative device structure. As mentioned previously, the bulk conduction shields the carriers from the kind of degradation they would suffer if the channel were at the surface; i.e., high surface fields and surface scattering that reduce

the mobility, and hot carrier injection into the oxide. In both the inversion and depletion modes, conduction occurs exclusively in the silicon bulk. Now, as V_G increases even further, and the surface depletion layer vanishes, a layer of electrons forms at the surface. This is known as the accumulation mode of operation and the conduction mechanism is similar to that in a SC MOSFET. Fig. 23 illustrates this mode of operation.

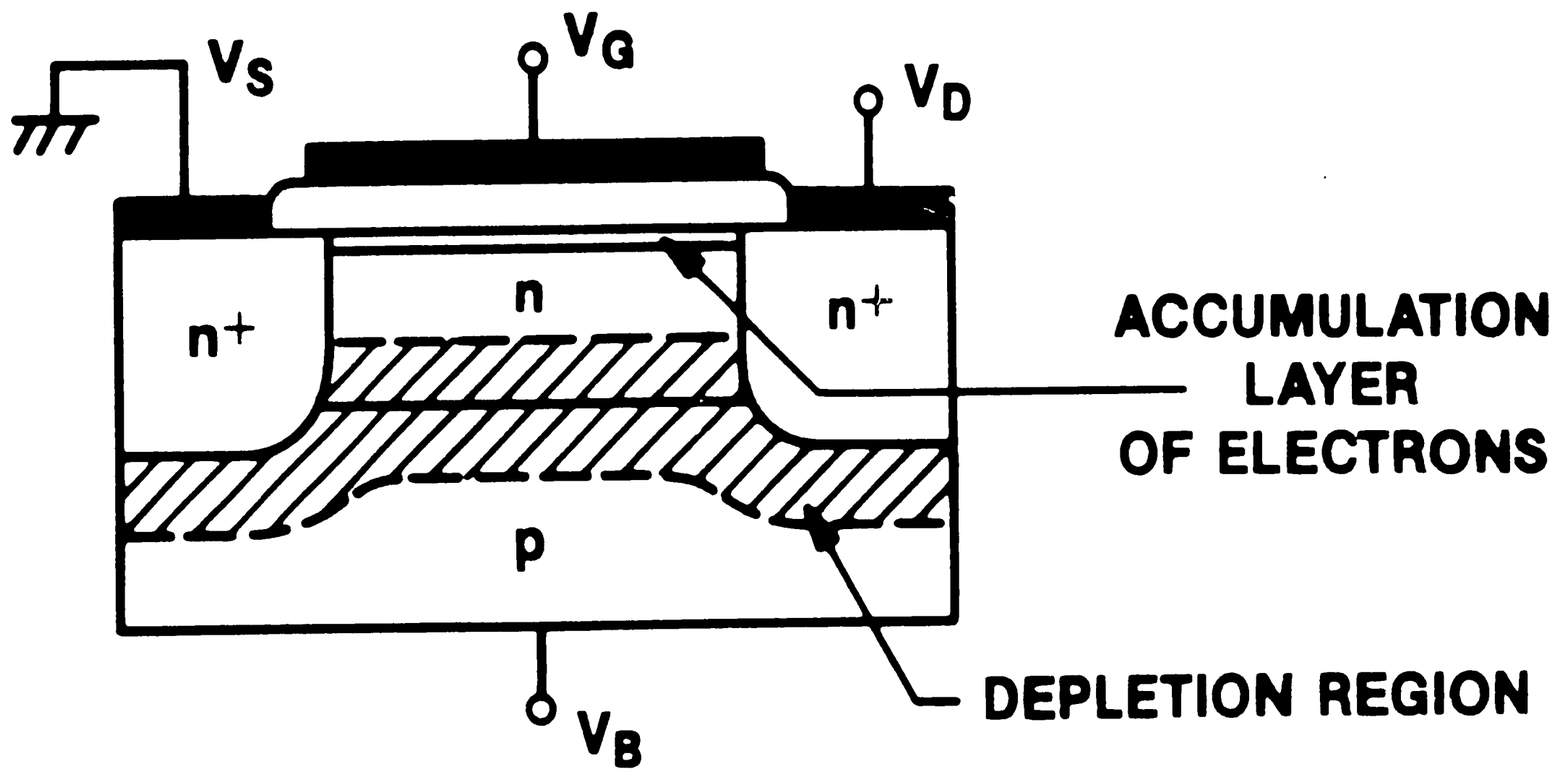


Figure 23. BC MOSFET Operated in the Accumulation Mode

In addition to these three basic modes of operation, two appropriate transition regions - partial accumulation, and depletion-inversion also occur. When a drain bias is applied, the channel does not form uniformly across the device. For example, the surface may appear to be in accumulation on one side and depletion on the other; or in inversion on one side and depletion on the other, depending on the gate potential.

Typical I-V characteristics for the BC DM device are shown in Figs. 24-25.

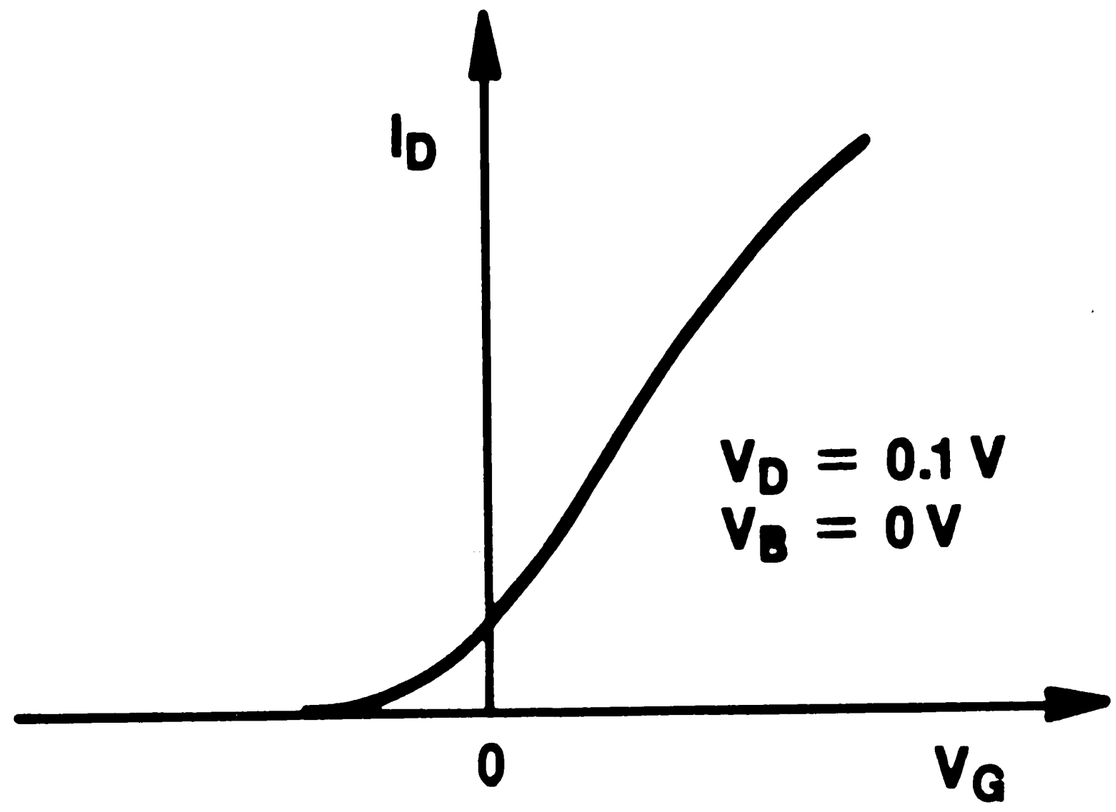


Figure 24. Threshold Characteristic of a BC DM MOSFET

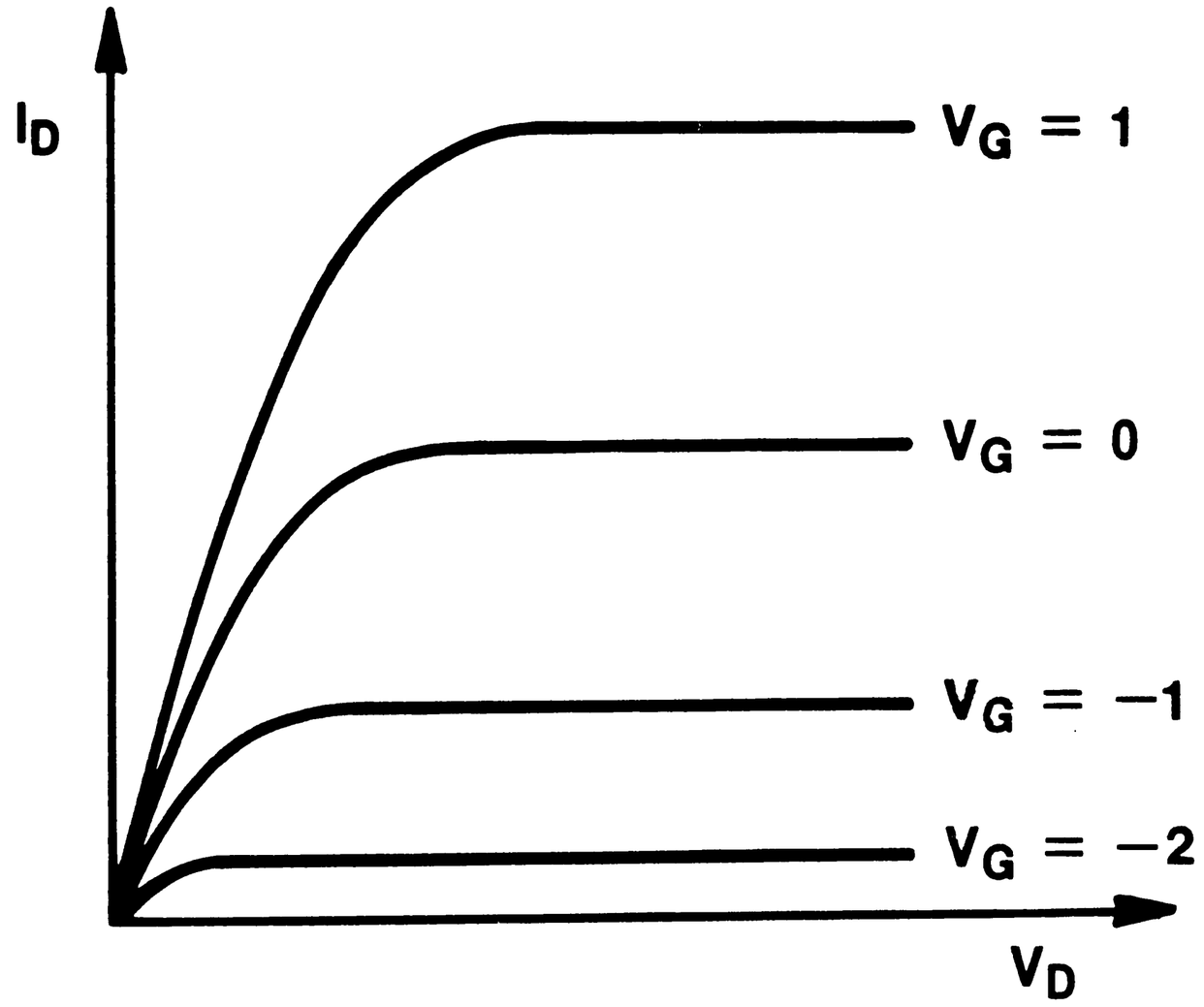


Figure 25. Output (Drain) Characteristic of a BC DM MOSFET

Physical device simulation can be used to explain the change in slope that appears to occur in the threshold characteristic at about $V_{GS} = 0.1$ volt for this particular device, as shown in Fig. 26. Plots of electron density in the channel just before and just after this "bump" are shown in Figs. 27 and 28. In these figures, the contour plots show lines of constant electron density where, for example, 16 equals 10^{16}, and the three-dimensional plot is viewed from the surface of the device. The majority of the current flows where the electron density is highest. Fig. 27 shows that a slight depletion region still exists near the surface, while, in Fig. 28, the accumulation of electrons at the surface is clearly identified and the density is above the doping level in the channel. From these plots, the change in slope can be identified as the onset of accumulation. In the accumulation mode, conduction occurs at the surface where the mobility is reduced, as in a SC device, due to the vertical field and surface scattering mechanisms; hence the change in slope.

To show that this is not just an artifact of the physical device simulator, the measured I-V curve of an actual BC device (NMOS $200\mu m$ x $200\mu m$) is shown in Fig. 29.

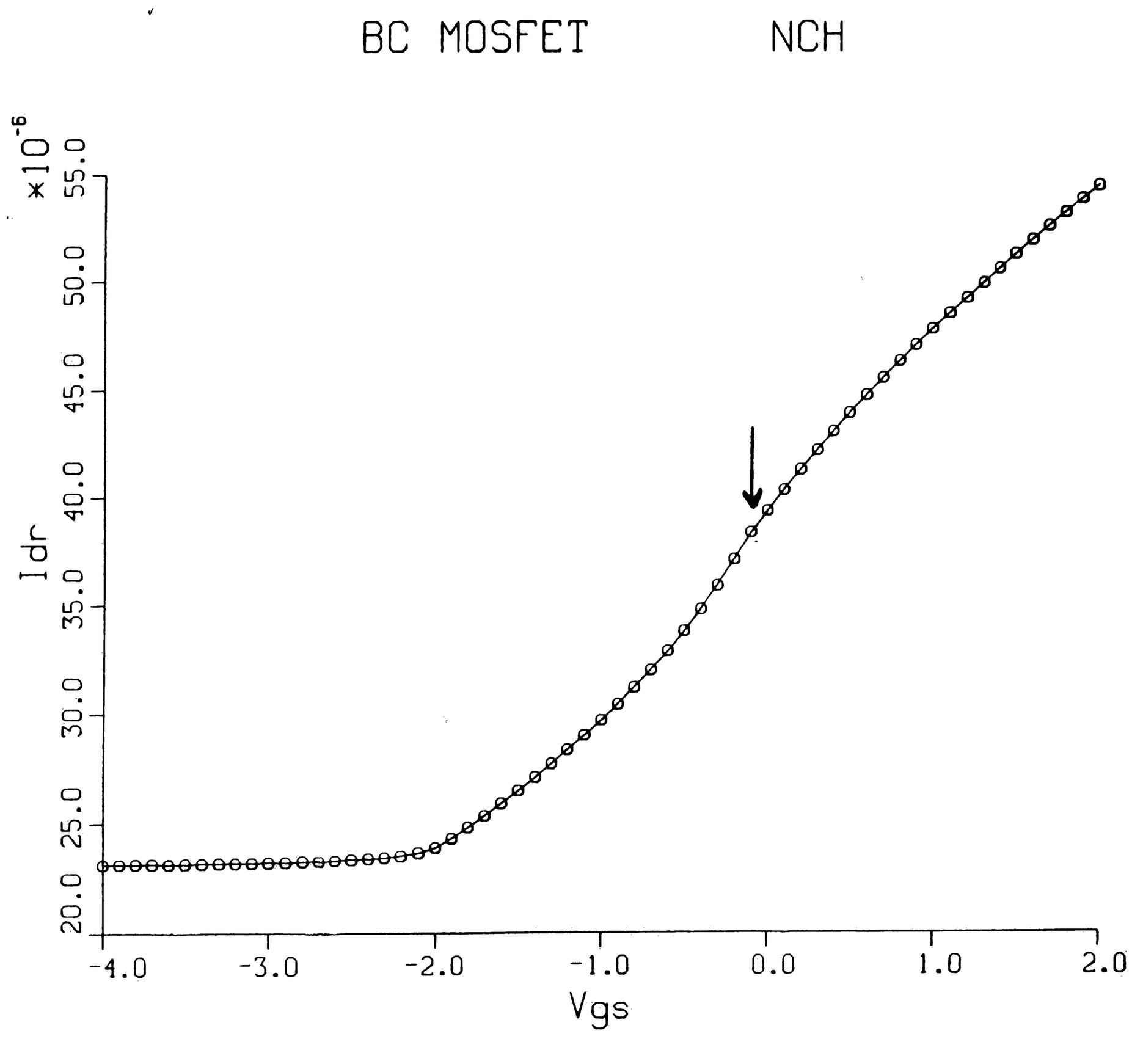


Figure 26. Simulated I-V Curve of a BC MOSFET

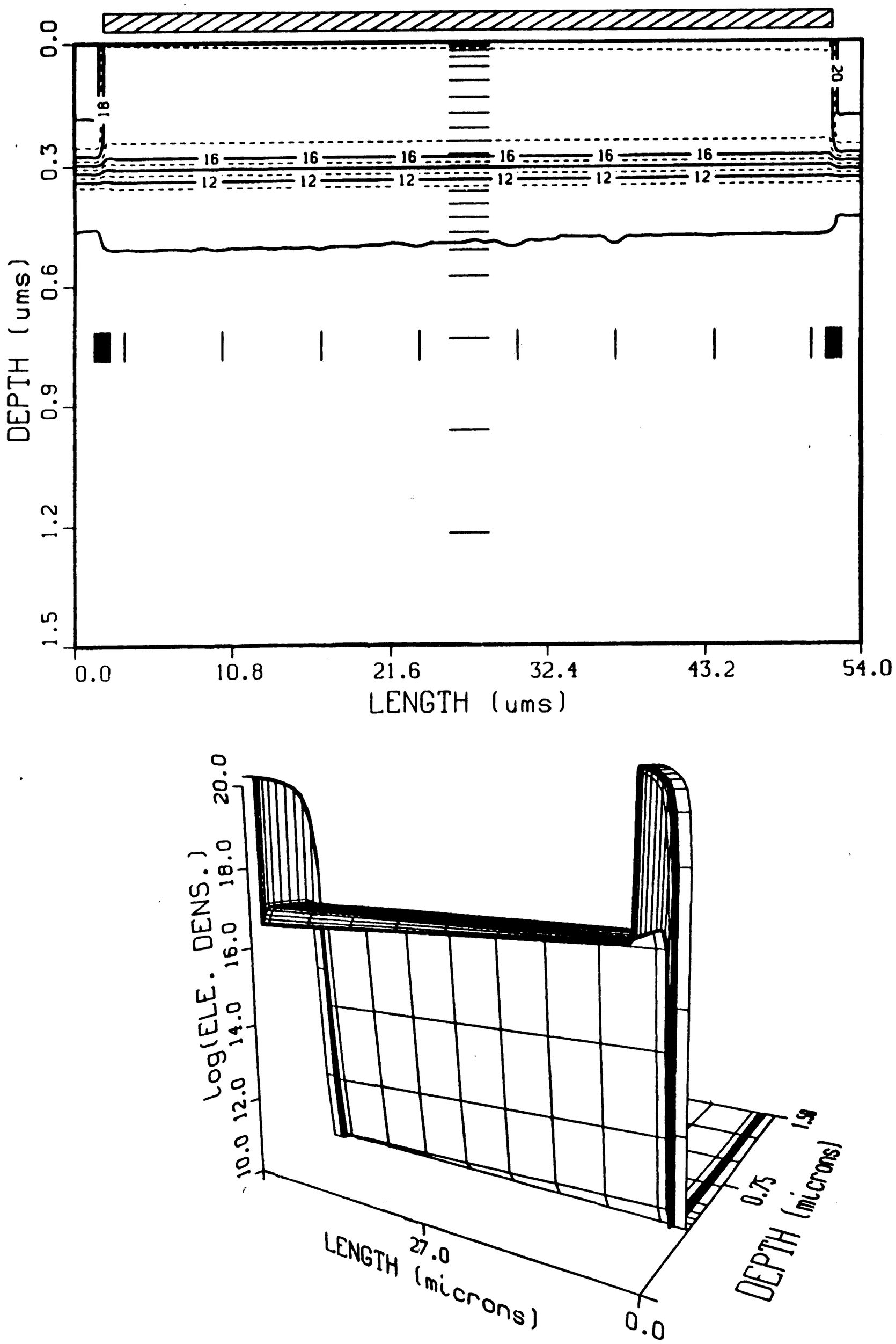


Figure 27. Electron Density of a BC MOSFET Just Before Accumulation

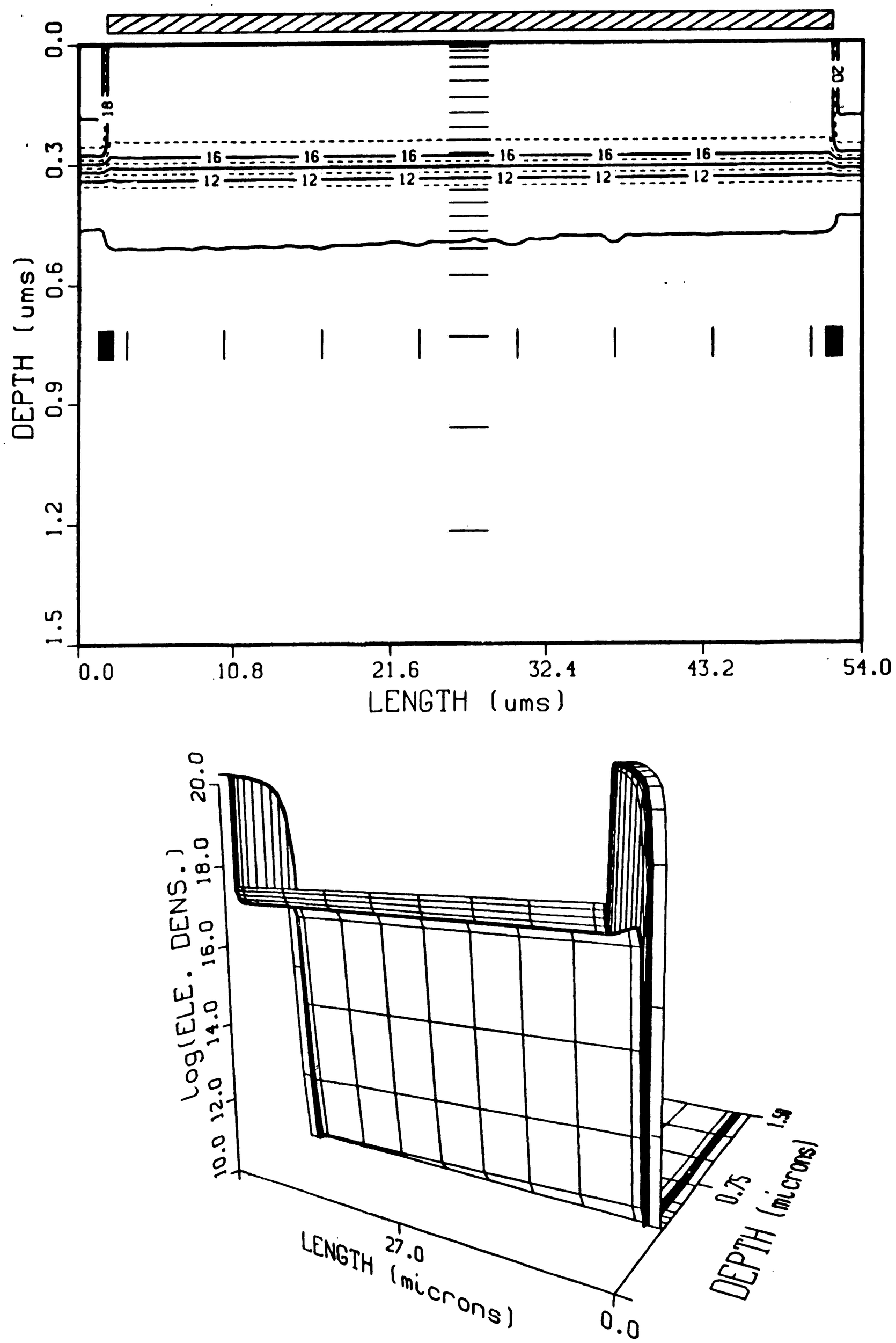


Figure 28. Electron Density of a BC MOSFET Just After the Onset of Accumulation

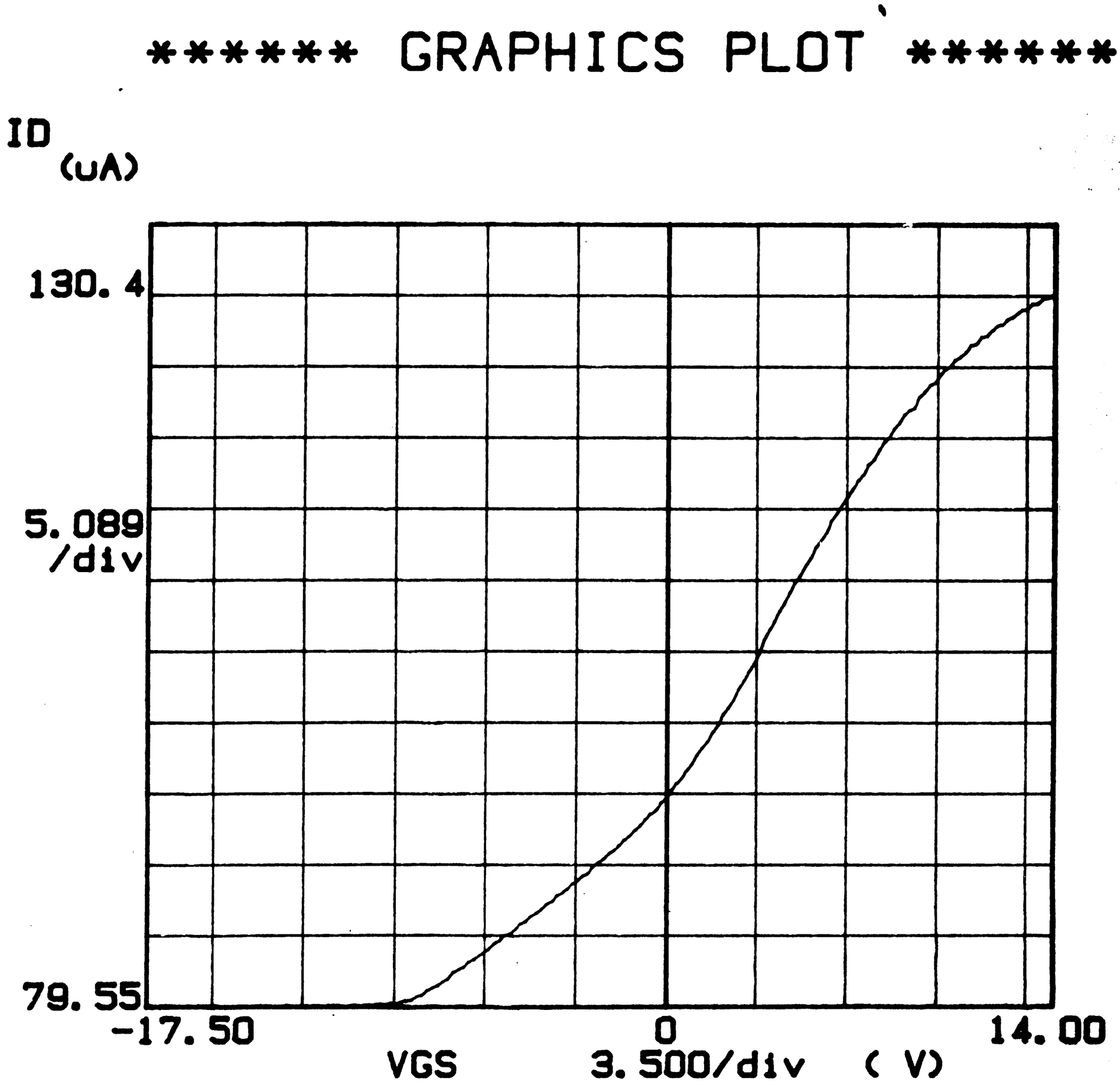


Figure 29. Measured I-V Curve of an Actual BC MOSFET

III. REVIEW OF MODELS

A. CSIM

For large geometry devices, the complete CSIM model is not necessary, therefore, an overview of the derivation of the first order model is given here. A cross section of a SC MOSFET with appropriate labels is shown in Fig. 30

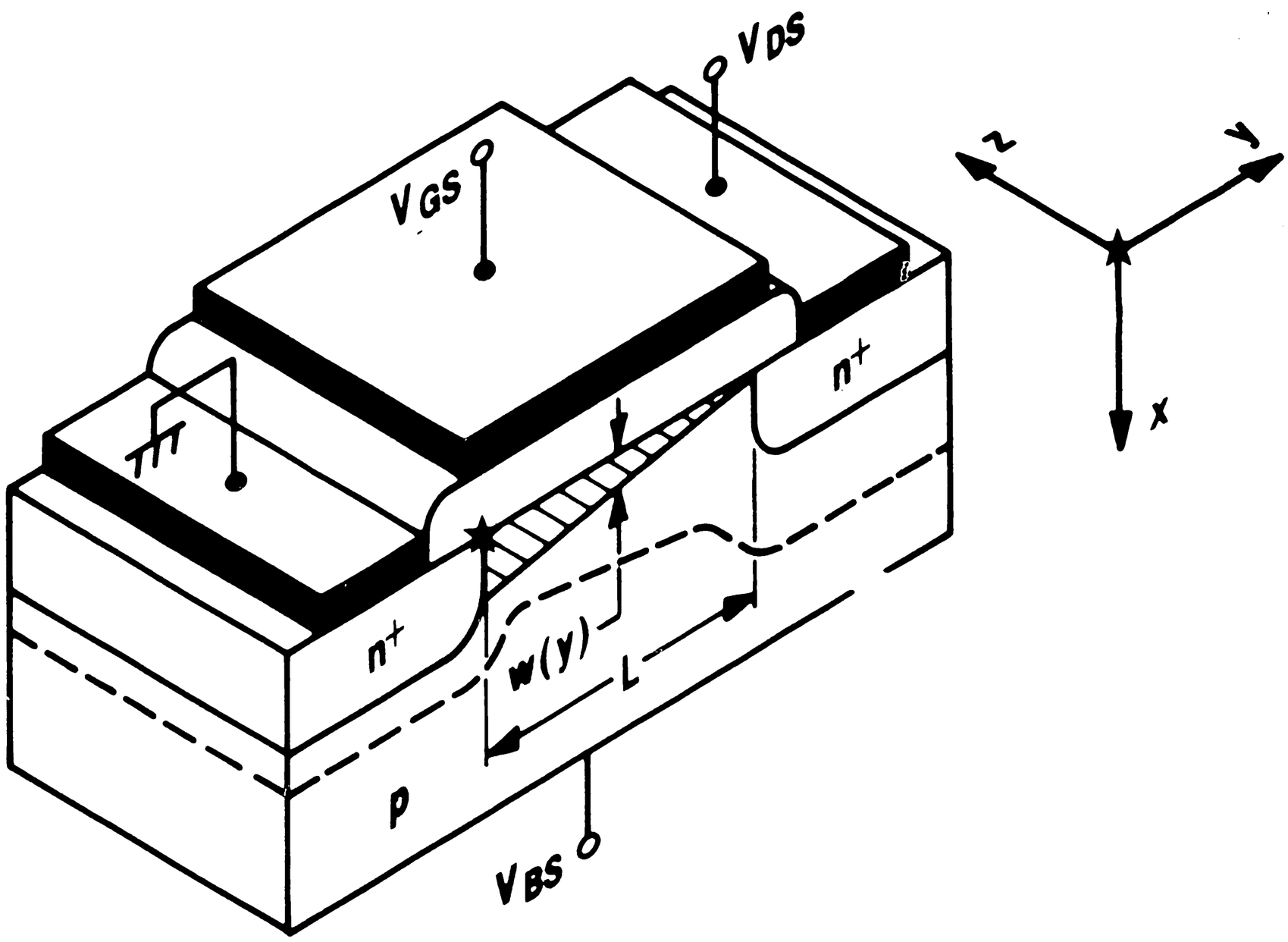


Figure 30. Cross Section of SC MOSFET

where

L = channel length

Z = channel width

$w(y)$ = width of inversion layer from Si-SiO_2 interface.

The approach used to obtain the drain current expression is basically that of Swanson[32]. A mathematically rigorous approach would involve the solution of the two-dimensional Poisson and continuity equations. However, in order to obtain a simple analytical solution, several approximations are necessary. As mentioned previously, the analysis is done for a long channel device, such that the channel length, L, is much longer than the sum of the source and drain depletion layer widths. Secondly, the gradual channel approximation is used; that is, the vertical or transverse component of the electric field, E_x, is much larger than the horizontal or longitudinal field, E_y. This approximation allows a one-dimensional analysis to be performed. Finally, current flow is assumed to be parallel to the surface, consisting of electrons carried by the drift process.

The current transport equation can be written as:

$$J_n = q\mu_n n \frac{d\phi_n}{dx} \tag{1}$$

where

J_n = electron current density

q = electronic charge

μ_n = electron mobility

n = electron density

ϕ_n = electron quasi-Fermi level.

An incremental section of the drain current is obtained by integrating (1) from 0 to $w(y)$.

$$I_{DS} = \int_0^{w(y)} Z J_n \, dx \tag{2}$$

Next, this equation is integrated over the channel to obtain the total drain current. To do this, the current is assumed to be constant, i.e., generation/recombination is negligible. Note that the left hand side is integrated from 0 to L, and the right hand side is integrated from 0 to V_D.

$$I_{DS} = q\frac{Z}{L}\int_0^{V_D} dV \int_0^{w(y)} \mu_n(x,V)N(x)dx \tag{3}$$

The complete derivation is beyond the scope of this thesis. However, the result leads to three regions of MOSFET operation which is the first order CSIM model:

Cutoff Region [$V_{GS} \leq V_T$]:

$$I_{DS} = 0. \tag{4}$$

Triode Region [$V_{GS} > V_T$ and $0 < V_{DS} < V_{SAT}$]:

$$I_{DS} = \beta_0 \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \, (1 + \lambda V_{DS}) \tag{5}$$

Saturation Region [$V_{GS} > V_T$ and $V_{DS} \geq V_{SAT}$]:

$$I_{DS} = \frac{\beta_0}{2}(V_{GS} - V_T)^2 \, (1 + \lambda V_{DS}) \tag{6}$$

The threshold voltage, V_T, is defined by:

$$V_T = V_{TO} + K_1\left[\sqrt{\phi_s - V_{BS}} - \sqrt{\phi_s}\right] \tag{7}$$

and the saturation voltage, V_{SAT}, is defined by:

$$V_{SAT} = V_{GS} - V_T. \tag{8}$$

Note that the subthreshold region of operation is not included in the CSIM model. Instead, the device is considered to be in a "cutoff" mode. In this model, then, the drain current is a function of three voltages: V_{GS}, V_{DS}, and V_{BS}, and five model parameters:

β_0, the transconductance parameter

K_1, the body-effect parameter

ϕ_s, the surface potential

V_{TO}, the zero-bias threshold voltage

λ, the channel-length modulation parameter.

These five parameters are in turn related to IC processing parameters by the following equations.

$$\beta_0 = \mu_s C_{OX}\frac{Z}{L} \tag{9}$$

$$K_1 = \frac{\sqrt{2qK_s\epsilon_o N_{SUB}}}{C_{OX}} \tag{10}$$

$$\phi_s = 2\phi_F = 2\frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right) \tag{11}$$

$$V_{TO} = V_{FB} + \phi_s + K_1\sqrt{\phi_s} \tag{12}$$

$$\lambda = \frac{1}{L}\left(\frac{2K_s\epsilon_o}{q\phi_s N_{SUB}}\right)^{1/2} \tag{13}$$

where

μ_s = surface mobility

$C_{OX} = \frac{K_o\epsilon_o}{T_{OX}}$ = oxide capacitance

K_o = dielectric constant of the oxide

ϵ_o = permittivity in vacuum

T_{OX} = oxide thickness

K_s = dielectric constant of silicon

N_{SUB} = substrate doping

V_{FB} = flat-band voltage.

In the first order CSIM model used here, μ_s reflects the "average" value of surface mobility over the range of operation. In the complete CSIM model, there is an additional term that accounts for the mobility reduction due to surface scattering. This is a key item in modeling SC devices but is not important when applying this model to the DM BC device.

B. BC Model

A cross section of a BC MOSFET with appropriate labels is shown in Fig.

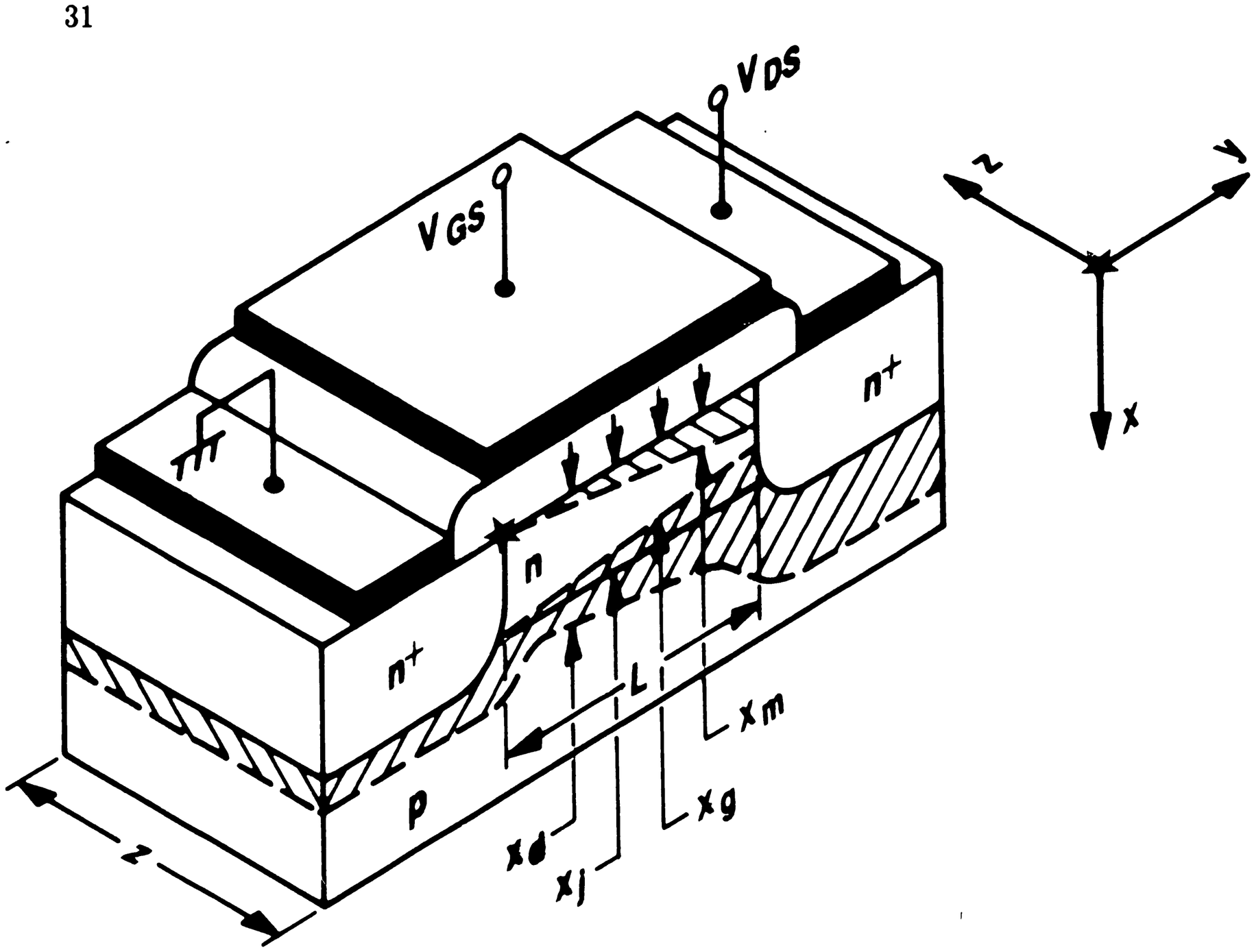


Figure 31. Cross Section of BC MOSFET

where

x_m = surface depletion width

x_g = upper edge of bulk depletion region measured from the S_i surface

x_d = lower edge of bulk depletion region.

To obtain an analytical expression for the drain current, it is necessary to make several approximations. In addition to those made for the CSIM model, which

are also valid here, the analysis is done only for the depletion-mode of operation. Also, the impurity densities are approximated by a step junction profile and the carrier mobility in the channel is assumed to be constant.

The same approach used for the CSIM model is followed here, except that the limits of integration used in equations (2) and (3) are different. The channel region for the BC model extends from x_m to x_g rather than from 0 to $w(y)$. Also the terms $\mu_n(x,V)$ and $N(x)$ are assumed to be constant and can be taken out of the integral. The resulting expression is:

$$I_{DS} = q\frac{Z}{L}\overline{\mu}_n \overline{N}_D \int_0^{V_D} [x_g(V_B,V) - x_m(V_G,V)]dV \tag{14}$$

Assuming an abrupt profile, p-n junction theory is used to evaluate the terms x_g and x_m. Integration is then straightforward.

The results obtained for the BC model are valid for the depletion-mode range of operation and only in the triode or linear region where the drain voltage is less than the saturation voltage. The current in this model is a function of three voltages: V_{GS}, V_{DS}, and V_{BS}, and five parameters: λ, β_0, γ, ϕ_B, and V_P.

$$I_{DS} = \frac{\beta_0\lambda}{1+\theta_C V_{DS}}\left[\frac{\lambda V_{DS}}{2} - g(V_{GS},V_{DS},V_P) - \gamma g(V_{BS},V_{DS},\phi_B)\right] \tag{15}$$

where

$$g(V_1, V_2, \xi) = \frac{2}{3}\left[(V_1 + V_2 + \xi)^{3/2} - (V_1 + \xi)^{3/2}\right] \tag{16}$$

The parameters are defined by the following expressions.

$$\lambda = \frac{\sqrt{2qK_s\epsilon_0 N_D}}{C_{eff}} \tag{17}$$

$$\beta_0 = \bar{\mu}_0 \left(\frac{Z}{L}\right) C_{eff} \tag{18}$$

$$\gamma = \left(\frac{\bar{N}_A}{\bar{N}_A + \bar{N}_D}\right)^{1/2} \tag{19}$$

$$\phi_B = \frac{kT}{q} \ln\left(\frac{\bar{N}_A \bar{N}_D}{{n_i}^2}\right) \tag{20}$$

$$V_P = \frac{qK_s\epsilon_0 \bar{N}_D}{2{C_{OX}}^2} - V_{FB} \tag{21}$$

where

$$C_{eff} = \frac{K_0\epsilon_0}{(T_{OX} + (K_0/K_s)x_j)} \tag{22}$$

x_j = the junction depth of the ion-implanted channel

$\bar{\mu}_0$ = bulk mobility in the channel

$\bar{N}_D$ = channel doping

$\bar{N}_A$ = substrate doping

The other terms have been defined previously for the CSIM model and have the same meaning here. It should be noted that the parameter V_P is not the same

as the pinch-off voltage, V_{PO}, defined on page 10 and that the parameter λ is not the same as the parameter λ in the CSIM model. Here, λ is equivalent to the CSIM parameter K_1, the body effect parameter, although the definition is somewhat different. Also, C_{eff} is an effective capacitance consisting of the oxide capacitance and the depletion capacitance of the channel region in series.

IV. EXPERIMENTAL RESULTS

A. Device Simulation

Profiles for a BC MOSFET, as obtained from BICEPS[4], a two-dimensional process simulation program used at AT&T Bell Labs, were shown previously in Figs. 7-9. This profile was altered as shown in Fig. 32 to obtain a step profile, thereby satisfying one of the assumptions of the BC model. Numerical integration of the actual profile, using the trapezoid rule, was used to obtain $\overline{N}_D$ and $\overline{N}_A$ such that

$$\overline{N}_D x_{j1} = \int_0^{x_{j1}} N_D(x)dx \tag{23}$$

and

$$\overline{N}_A(x_{j2}-x_{j1}) = \int_{x_{j1}}^{x_{j2}} N_A(x)dx \tag{24}$$

The junction depths x_{j1} and x_{j2} are indicated on Fig. 32 and the resulting values obtained were $\overline{N}_D = 1.2\text{x}10^{17}/cm^3$ and $\overline{N}_A = 9.7\text{x}10^{15}/cm^3$. This method is preferred over an analytical method where $N(x)$ is estimated with a gaussian function. As can be observed in Fig. 32, the actual profile is not truly gaussian due to the thermal steps in the process that follow the ion implantation.

This step profile was used as input to MEDUSA, a two-dimensional device simulator, to obtain the device characteristics for a $50\mu m$ x $50\mu m$ n-channel device. These characteristics are calculated by solving the Poisson and

continuity equations in two dimensions, and are used to verify the model after parameters have been extracted.

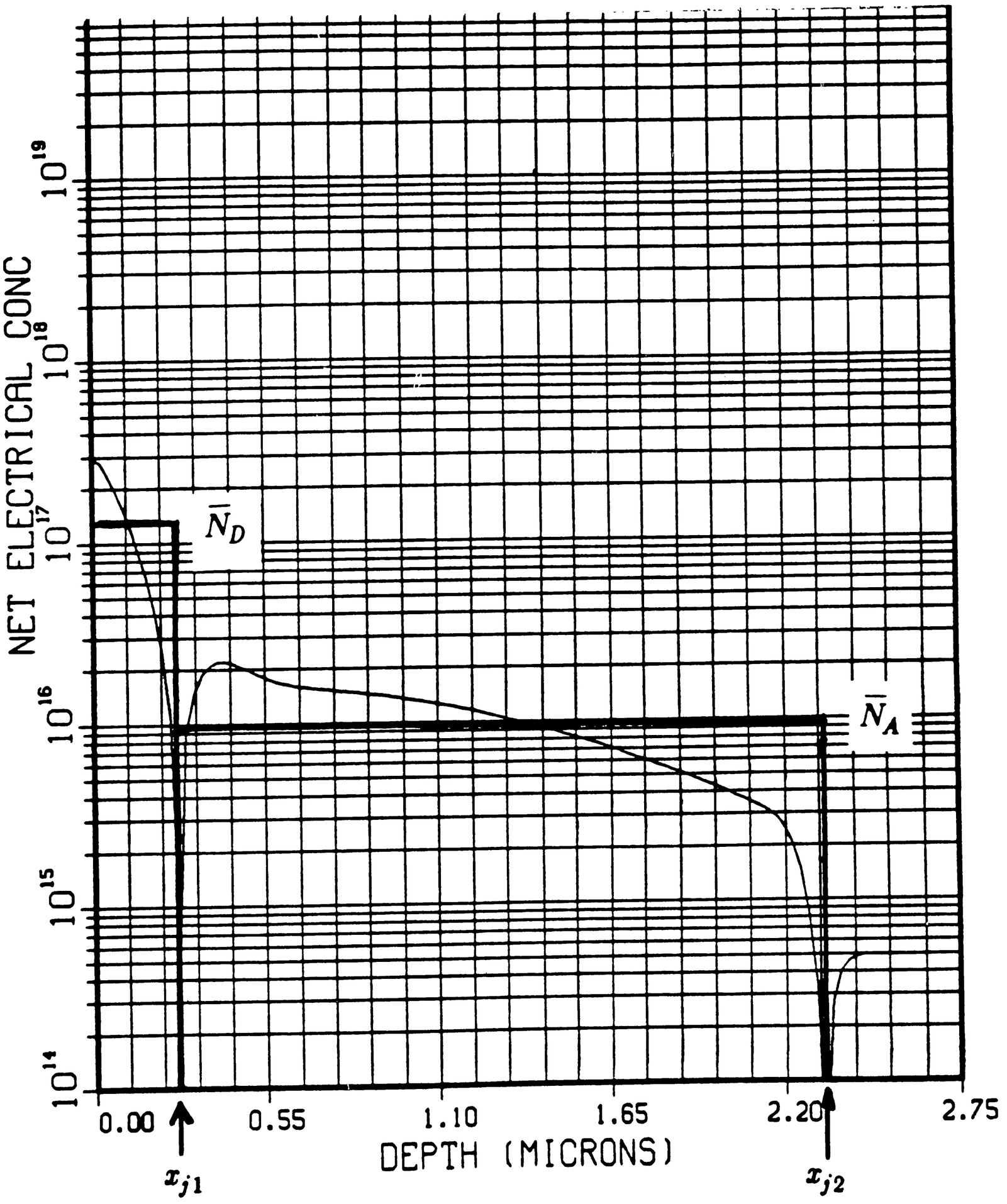


Figure 32. Approximation of Device Profile

B. Parameter Extraction

1. CSIM

All parameters for the CSIM model are obtained by using MOSPAC[2], a software package for parameter extraction. Input to MOSPAC is a set of "threshold voltages" at various values of V_{BS}, and a set of drain characteristics (I_{DS} *vs.* V_{DS}) at various gate voltages. The "threshold voltages" are obtained from the extrapolated intercept of the I_{DS} *vs.* V_{GS} curves. The algorithm in MOSPAC is based on a non-linear least squares fit to these data. The resulting set of parameters extracted for the $50\mu m$ x $50\mu m$ device are shown in Table 1, along with the expected values. These expected values are calculated from the known inputs to MEDUSA using equations (9)-(13).

Parameter	Extracted Value	Expected Value	Unit
β_0	$4.969\text{x}10^{-5}$	$1.48\text{x}10^{-4}$	$amp/volt^2$
K_1	1.453	0.2876	$volt^{½}$
ϕ_s	0.8651	0.7127	$volt$
V_{TO}	-6.103	0.36	$volt$
λ	0.0	0.0	$volt^{-1}$
μ_s	251.8	750.0	$cm^2/volt \cdot sec$
N_{SUB}	$2.48\text{x}10^{17}$	$9.7\text{x}10^{15}$	cm^{-3}

TABLE 1. CSIM Parameters

Electron mobility is a function of impurity concentration and since the simulated device has a constant value of $\overline{N}_D = 1.2\text{x}10^{17}/cm^3$ in the channel, the mobility in the channel can be obtained from a plot of mobility vs. impurity

concentration[33], as shown in Fig. 33. The IC processing parameters, μ_s and N_{SUB}, calculated from the model parameters β_0 and K_1 using equations (9)-(10) are also shown in Table 1. Alternatively, N_{SUB} can be calculated from model parameter ϕ_s using equation (11), which results in a value of $1.85\text{x}10^{17}/cm^3$. This value is inconsistent with the value shown in Table 1.

MOSPAC results indicate an rms error of 5.4% in the fit to the drain characteristics for this device. This indicates that even though the parameter values are not close to the expected values, it is possible to match the device characteristics with the CSIM equations. It should be recalled that that only the first order CSIM model is used here. Several additional parameters can be extracted for the full CSIM model to improve the fit and to account for other effects, eg. short channel.

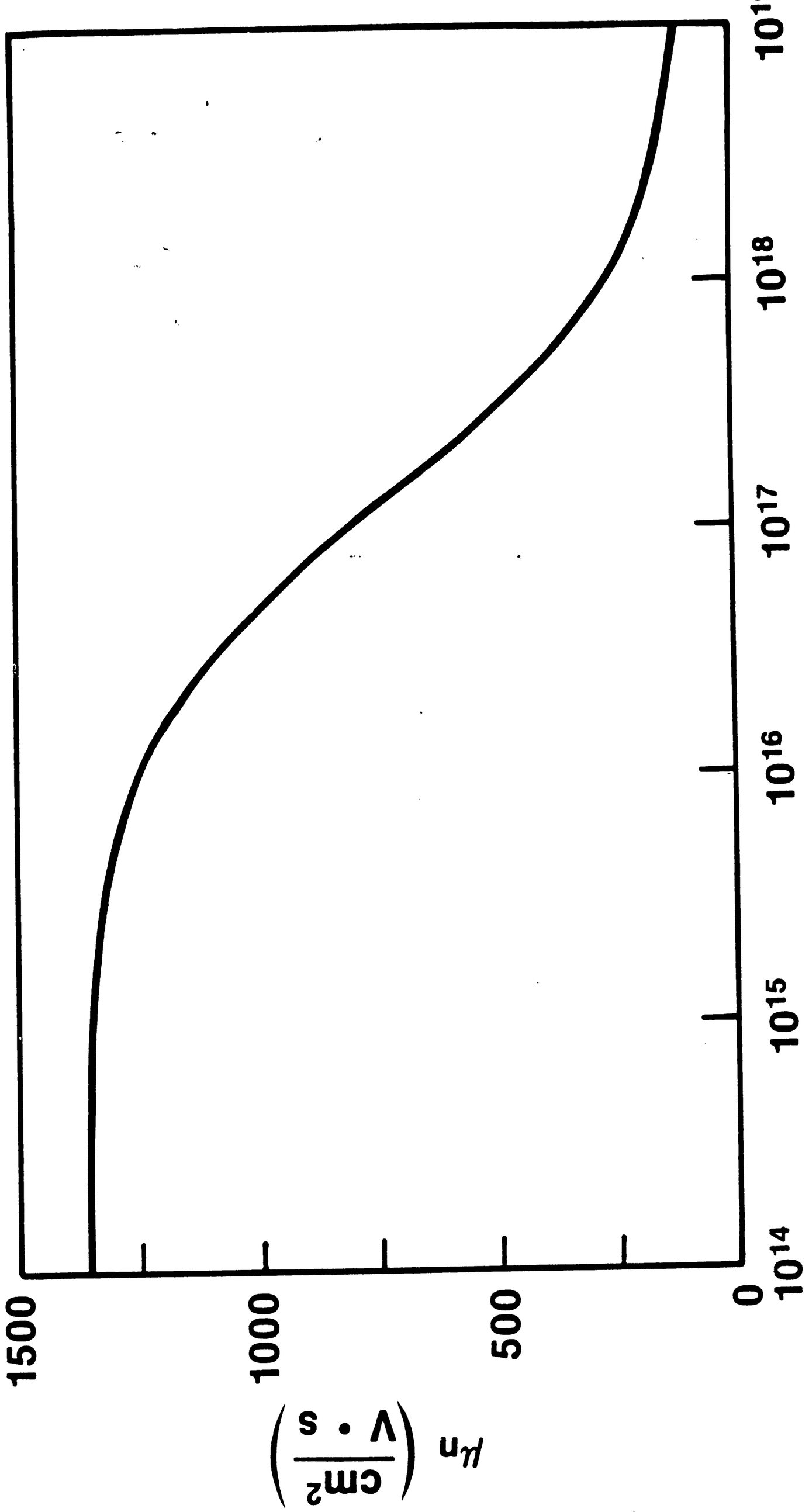


Figure 33. Electron Mobility vs. Impurity Concentration in n-Type S_i

2. BC Model

An analytical approach is used to extract parameters for the BC model, by formulating expressions for the conductances. With this technique, all the parameters can be obtained from three plots[3].

First, an expression for the transconductance with respect to the gate voltage, g_{mG}, is obtained in the depletion mode at small V_{DS}. Using equations (15)-(16), it can be shown that

$$g_{mG} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-\beta_0 \lambda V_{DS}}{2\sqrt{V_{GS} + V_P}} \tag{25}$$

or

$$g_{mG}{}^{-2} = \frac{4}{(\beta_0 \lambda V_{DS})^2}(V_{GS} + V_P) \tag{26}$$

Next, a plot of $g_{mG}{}^{-2}$ vs. V_{GS} is made as shown in Fig. 34. When $g_{mG}{}^{-2} = 0$ in equation (26), $V_{GS} = -V_P$ as indicated. Also, the slope is a function of $\overline{N}_D$; β_0 is a function of $\overline{\mu}_0$ which is a function of $\overline{N}_D$ as shown in Fig. 34, and λ is a function of $\overline{N}_D$ from equation (17).

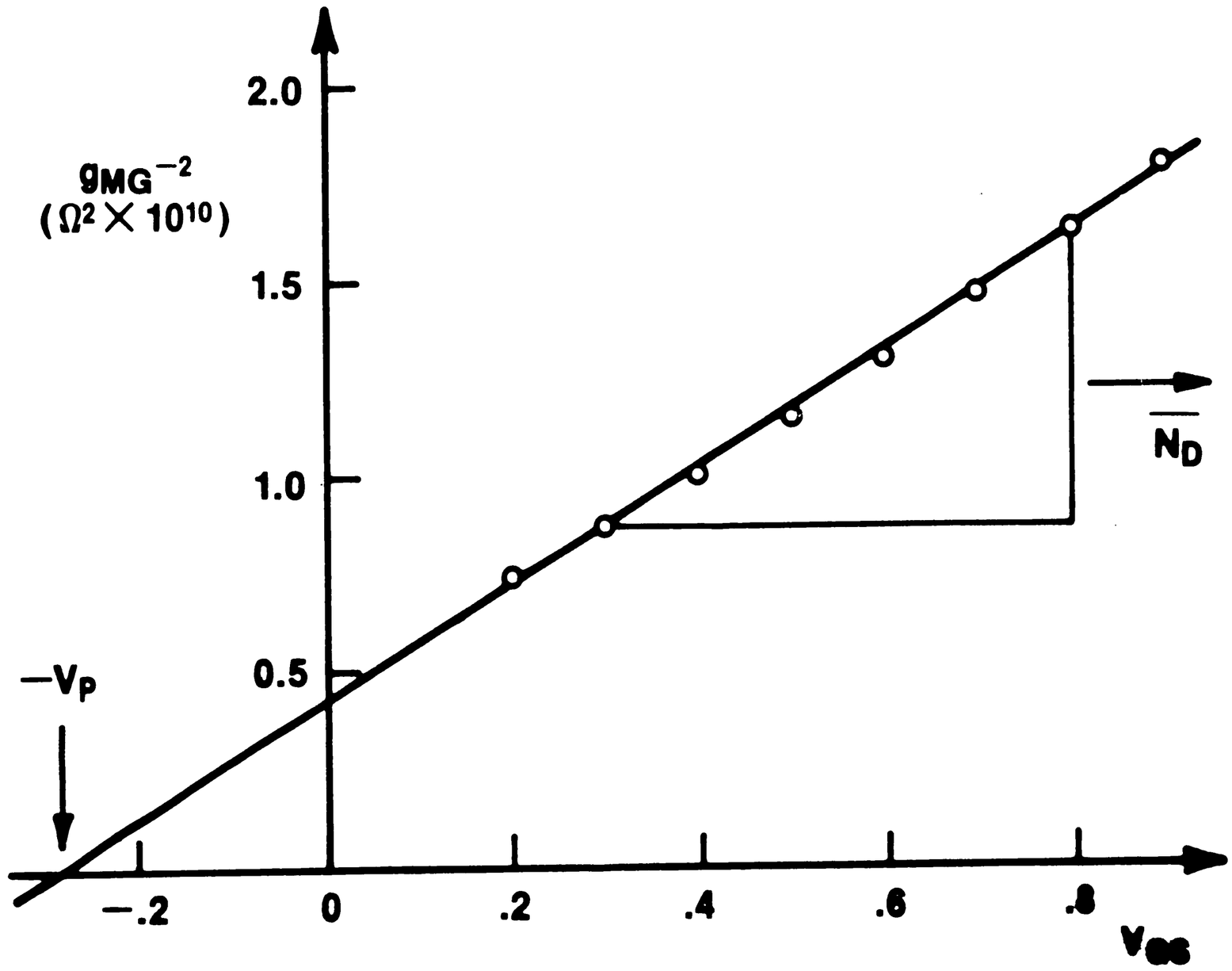


Figure 34. Extraction of $\overline{N}_D$ and V_P

Next, an expression for the transconductance with respect to the backgate voltage, g_{mB}, is obtained in the depletion mode at small V_{DS}. Using equations (15)-(16):

$$g_{mB} = \frac{\partial I_{DS}}{\partial V_{BS}} = \frac{-\beta_0 \lambda \gamma V_{DS}}{2\sqrt{V_{BS} + \phi_B}} \tag{27}$$

or

$$g_{mB}{}^{-2} = \frac{4}{(\beta_0 \lambda \gamma V_{DS})^2}(V_{BS} + \phi_B) \tag{28}$$

A plot of $g_{mB}{}^{-2}$ vs. V_{BS} is made as shown in Fig. 35. When $g_{mB}{}^{-2} = 0$ in equation (28), $V_{BS} = -\phi_B$ as indicated. In this case, the slope is a function of $\frac{\overline{N}_A \overline{N}_D}{\overline{N}_A + \overline{N}_D}$, due to the dependence on both γ and λ. Since $\overline{N}_D$ has been determined from the previous graph, it is straightforward, then, to solve for $\overline{N}_A$.

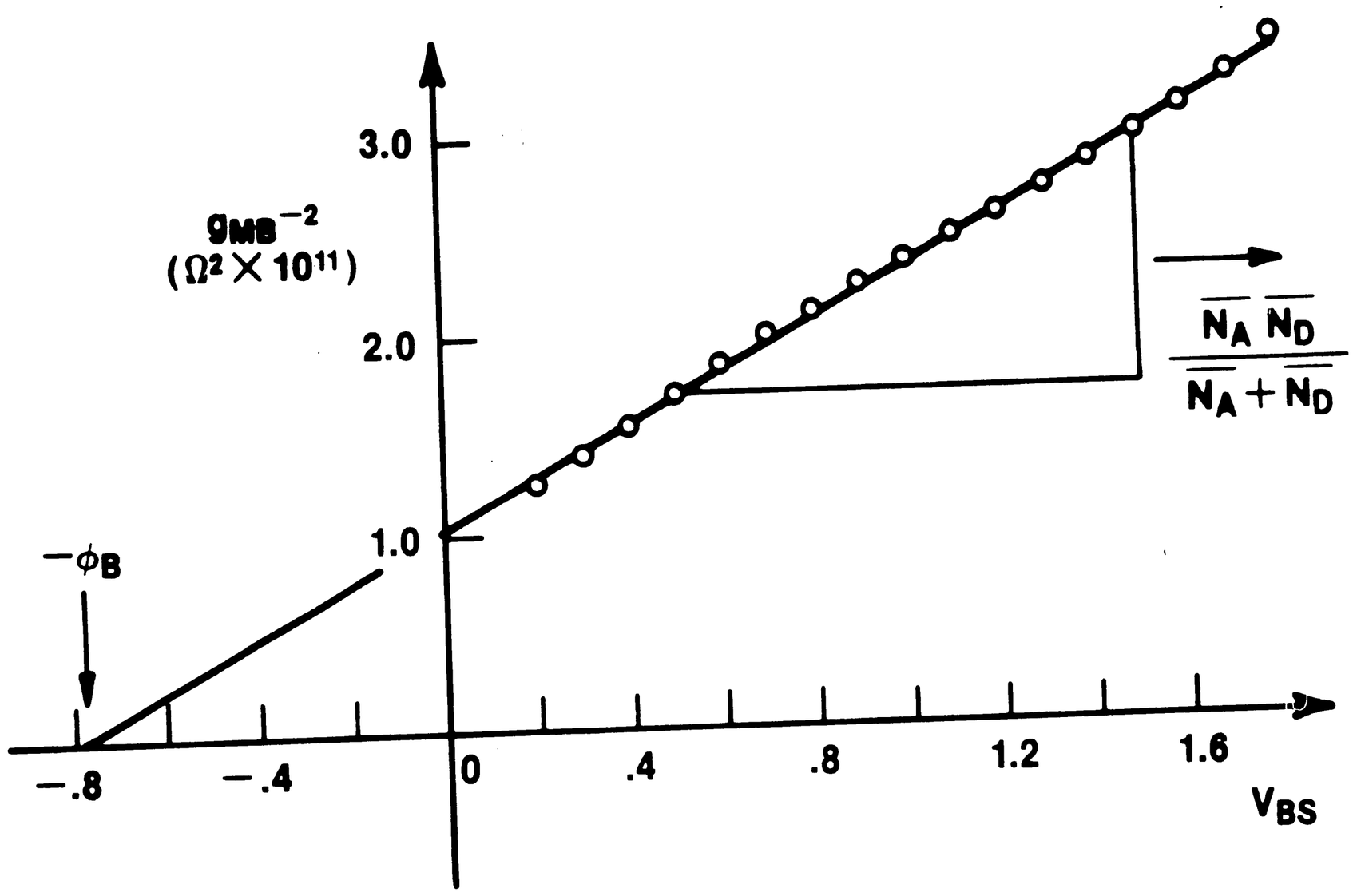


Figure 35. Extraction of $\overline{N}_A$ and ϕ_B

The junction depth of the implanted region, x_j, can be obtained by calculating the drain conductance, g_{D0}, under the condition of surface

inversion[31]. When the surface becomes inverted, x_m reaches its maximum value and equation (14) can be reevaluated. The following result is obtained:

$$g_{D0} = q\bar{\mu}_0 \frac{Z}{L} \bar{N}_D \left[x_j - (1+\gamma) \left(\frac{2K_s \epsilon_0}{q\bar{N}_A} [V_{BS} + V_{DS} + \phi_B] \right)^{1/2} \right] \tag{29}$$

Finally, x_j can be calculated from the y-intercept of the plot g_{D0} vs. $\sqrt{V_{BS} + V_{DS} + \phi_B}$, as shown in Fig. 36.

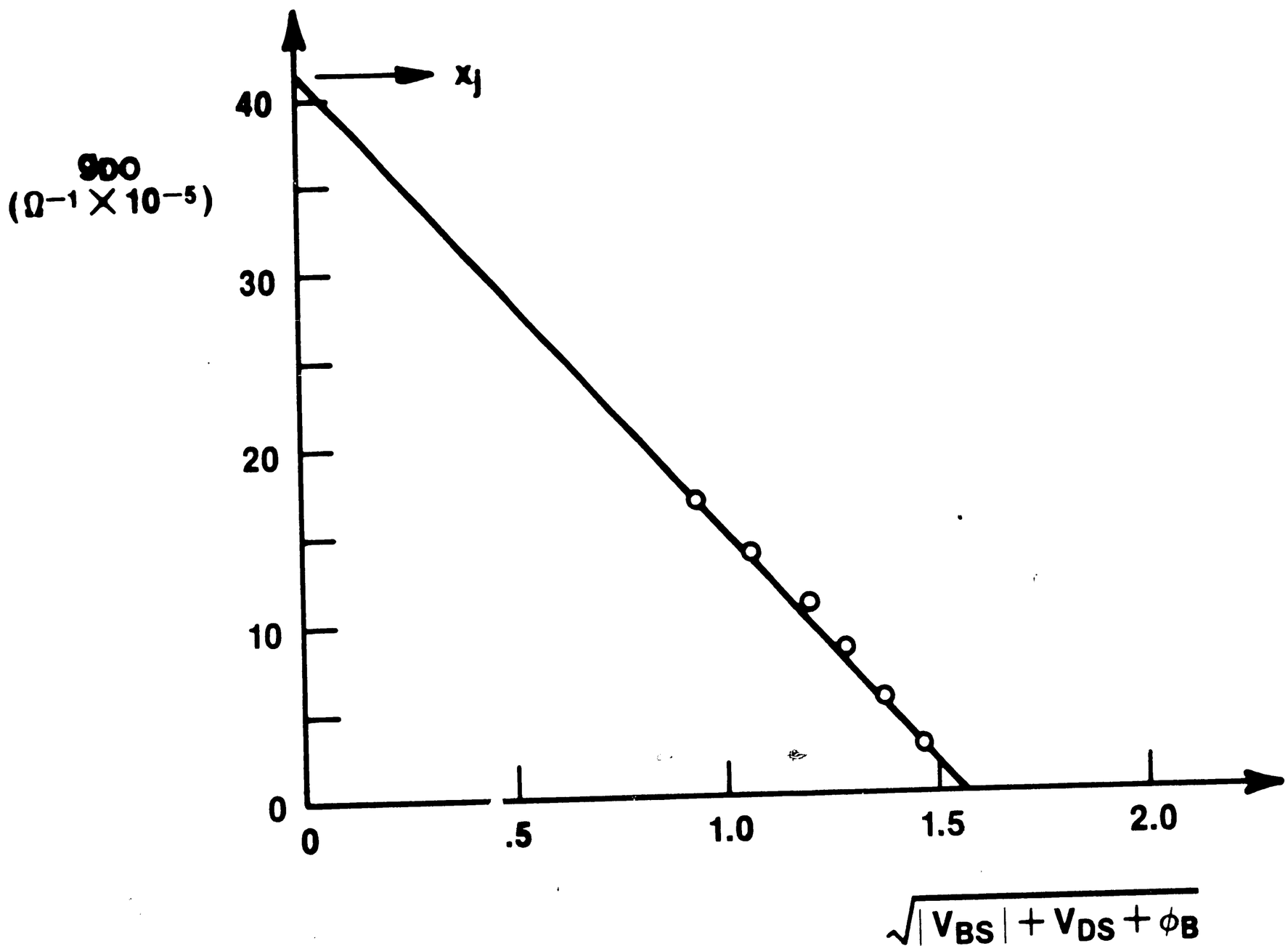


Figure 36. Extraction of x_j

Equations (17)-(22) are used to calculate the set of model parameters for the $50\mu m$ x $50\mu m$ device. The extracted and expected values of model parameters, as well as the IC processing parameters, $\overline{N}_D$, $\overline{N}_A$, $\overline{\mu}_0$ and x_j, obtained from Figs. 34-36, are given in Table 2.

Parameter	Extracted Value	Expected Value	Unit
λ	6.16	6.29	$volt^{½}$
β_0	$2.6\text{x}10^{-5}$	$2.4\text{x}10^{-5}$	$amp/volt^2$
γ	0.298	0.273	—
ϕ_B	0.78	0.778	$volt$
V_P	0.28	0.42	$volt$
$\overline{N}_D$	$1.3\text{x}10^{17}$	$1.2\text{x}10^{17}$	cm^{-3}
$\overline{N}_A$	$1.27\text{x}10^{16}$	$9.7\text{x}10^{15}$	cm^{-3}
$\overline{\mu}_0$	750.0	750.0	$cm^2/volt\cdot sec$
x_j	$2.59\text{x}10^{-5}$	$2.75\text{x}10^{-5}$	cm

TABLE 2. BC Model Parameters

Very good agreement between the extracted and expected parameter values is observed. This implies that the BC model is more physically based than CSIM when applied to the BC DM device. In addition, an rms error of 4.2% is obtained in the fit to the device I-V characteristics obtained from MEDUSA when the extracted values are used in the model equations.

C. Comparison of I-V Characteristics

The calculated drain characteristics for each model along with those predicted by MEDUSA are compared in the triode region of operation, since this is the only region in which the BC model can be applied[3]. A simple program was written to calculate the current for each model over a supplied voltage range and for a given set of model parameters. Figs. 37 and 38 show these results at two different backgate biases, $V_{BS} = 0$, and $V_{BS} = -5$, respectively. The marked points are data as simulated with MEDUSA, while the solid curves are calculated from the model parameters for the indicated models. At $V_{BS} = 0$, both models fit the data well, with an rms error of 5.4% for CSIM and 4.2% for the BC model. Four values of gate voltage are plotted: $V_{GS} = -0.1, -0.5, -1.0$, and -1.5. However, at $V_{BS} = -5$, the CSIM model greatly underpredicts the current. In Fig. 38, only the extremes in gate voltage are plotted: $V_{GS} = -0.1$ and -1.5. The rms error for CSIM is about 22% while only 4.9% for the BC model. It should be noted that parameter extraction for both models was done at $V_{BS} = 0$ and therefore optimized for that value. Since the BC model is more physically based for the BC device, a change in backgate voltage is accounted for correctly by the model equation. The parameters for the CSIM model are obtained by curve fitting and tend to lose their physical significance. It may be possible to get a better fit at $V_{BS} = -5$ if the parameters were extracted for that data.

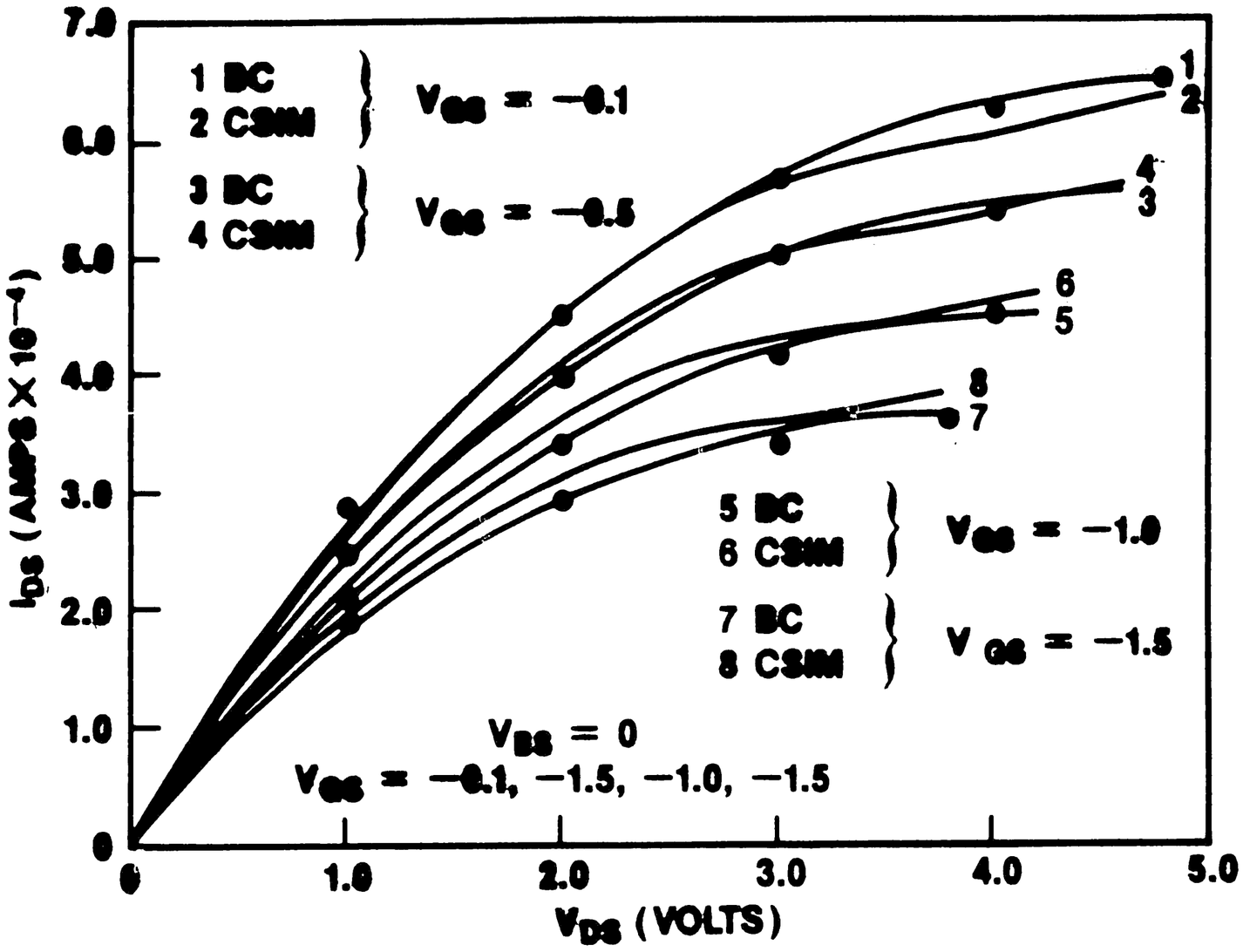


Figure 37. Comparison of Drain Characteristics at $V_{BS} = 0$

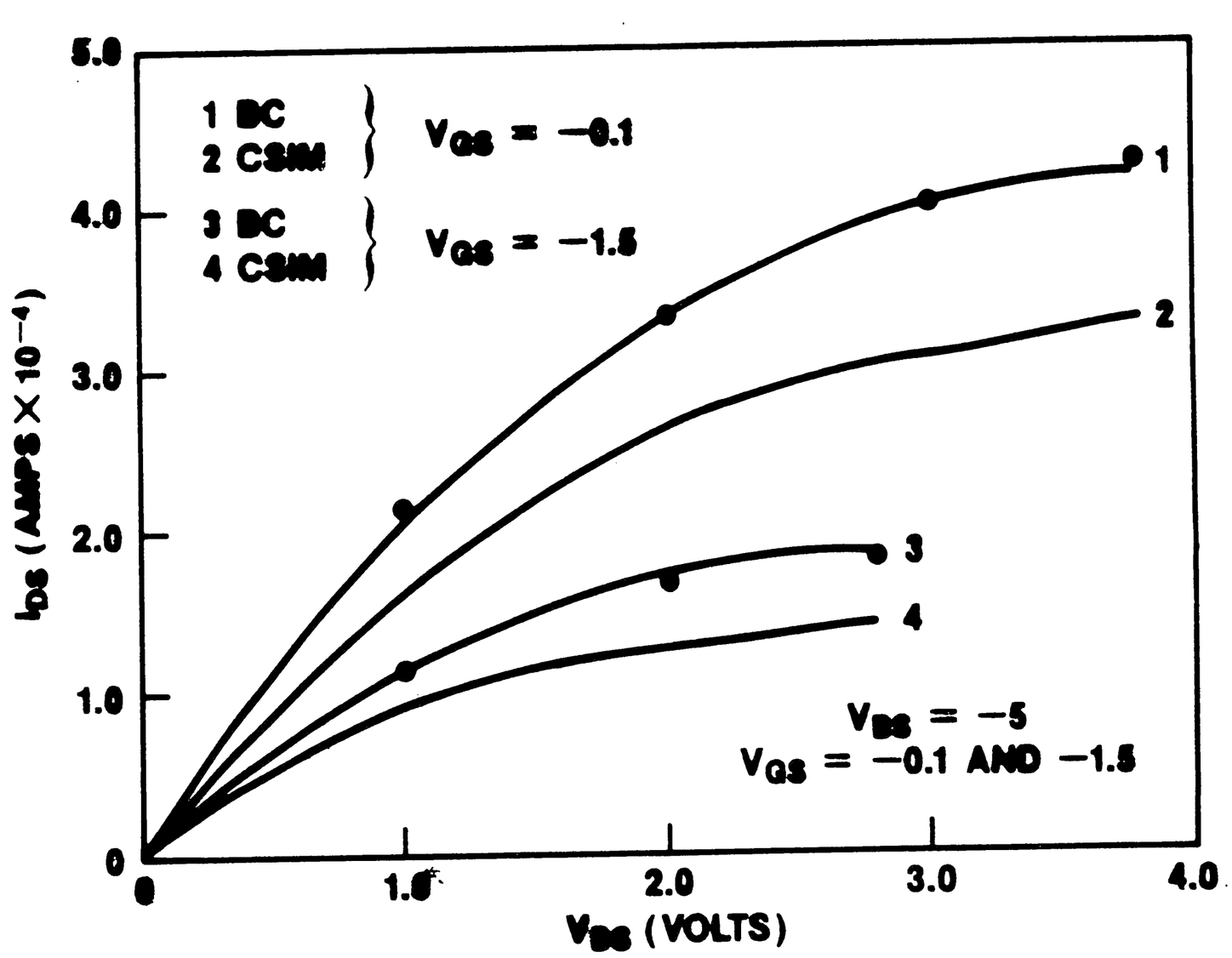


Figure 38. Comparison of Drain Characteristics at $V_{BS} = -5$

V. CONCLUSION

From the results of the last section, it has been shown that both models fit the device characteristics within reasonable accuracy over the range of operation where the models can be applied and in the range of substrate bias that was used to determine the parameters. Furthermore, the buried-channel model also correctly predicts the device behavior as a function of substrate bias. In addition, the parameters that can be related to IC process parameters, such as doping concentration and mobility, correspond much more closely to the values given to the device simulator in the case of the buried-channel model. This suggests that there may be merit in pursuing the development of a complete model for the buried-channel device. It also suggests that caution should be used when characterizing depletion-mode buried-channel devices with a surface type model. Although a reasonable fit can be obtained, the parameters lose their physical significance and are merely coefficients in the modeling equation.

Finally, some suggestions for future work are offered. The buried-channel model examined here, applies only in the triode region for a buried-channel depletion-mode MOSFET. As cited previously, some work has been done in extending the modeling to include other regions of operation. In addition, only large geometry devices have been considered. Some work has already been done[34],[35] to include small geometry effects. Little work, however, has been done in characterizing the "sub-pinch-off" region, which can be important for low voltage circuits and for the calculation of holding times in memory circuits.

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